INTEGRATED CIRCUITS

DATA HANDBOOK

Advanced Low-power Schottky (ALS) Logic Series

BOOK IC05 1989

Philips Components

PHILIPS

ADVANCED LOW-POWER SCHOTTKY (ALS) LOGIC SERIES

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Preface

Signetics would like to thank you for your interest in our ALS Product Family. Advanced Low–Power Schottky (ALS) can provide a system designer with enhanced speed and power performance, improved system reliability, and pin–for–pin compatibility with existing LSTTL.

Each data sheet contained in this data manual is designed to stand alone and reflect the latest DC and AC specifications for a particular device. Each 74ALS product is specified over a 10% V_{CC} range, for both AC and DC parameters.

This data manual includes:

- A Function Selection Guide
- A Circuit Characteristics Section
- A Users' Guide
- An application note covering Test Fixtures for High–Speed Logic
- A section on Surface Mounted ICs
- A section on Package Outlines

In addition to ALS, Signetics offers the broadest line of commercially available Logic Products, spanning a wide speed/power spectrum from ECL (100K/10K) to TTL (74, 74LS, 74S, 74F, 8T and 8200) to CMOS (4000 Series, 74HC/HCT, 74AC/ACT). Information on these product lines is also available from your nearest Signetics Sales Office, sales representative, or authorized distributor.

Product Status

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Package Outlines for Hermetic CERDIP . . . .
D **Plastic Small Outline** . . . .
N **Plastic Standard Dual–In–Line** . . . .

74ALS TTL Introduction

ADVANCED LOW–POWER SCHOTTKY PRODUCTS

FEATURES

- **5ns propagation delays**
- **1.2 mW/gate power dissipation**
- **Guaranteed AC performance over temperature and extended V_{cc} Range: 5V ± 10%**
- **High–impedance PNP base input structure for reduced bus loading in Low state**
- **Standard TTL functions and pinouts**
- **Replacement for LS types are $^{1}/_{2}$ the power and twice the speed.**
- **2KV ESD Protection**

PRODUCT DESCRIPTION

Signetics has combined advanced oxide–isolated fabrication techniques with standard TTL functions to create it's ALS product line. Low input loading allows the user to mix LS, FAST and HCMOS in the same system without the need for translators and restrictive fanout requirements.

ALS circuits are pin–for–pin replacements for LS types, but offer dissipation 2 to 3 times lower, and higher operating speeds. Existing systems can achieve much lower power and improved performance by replacing the LS types with the corresponding ALS devices.

The input structure provides better noise immunity due to higher thresholds, while the oxide–isolation and new circuit techniques create devices that have less variation with temperature or supply voltage than existing TTL logic families. Signetics guarantees all AC parameters under realistic system conditions – across the supply voltage spread and the temperature range, and with heavy 50_{p}F output loads.

Clamping diodes have been added to both the inputs and outputs to prevent negative overshoots. High input breakdown voltages allow unused inputs to be tied directly to V_{cc} without pull up resistors.

Multiple sources and a family of powerful circuits make Signetics ALS a wise TTL choice.

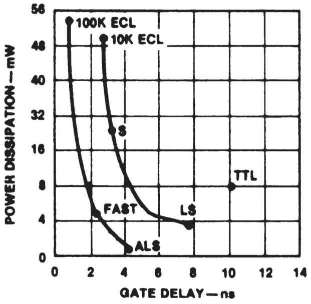

Figure 1. The Speed/Power Spectrum

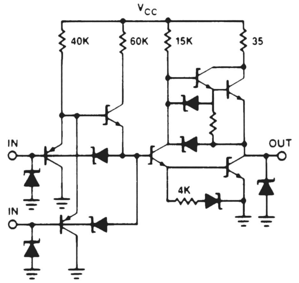

Figure 2. Basic ALS Gate

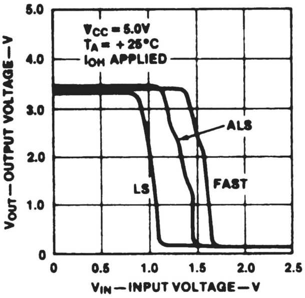

Figure 3. Transfer Functions At Room Temperature

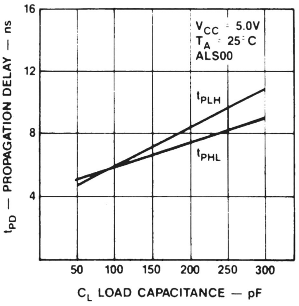

Figure 4. Propagation Delay VS Load Capacitance

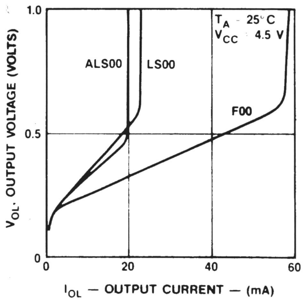

Figure 5. Output LOW Characteristics

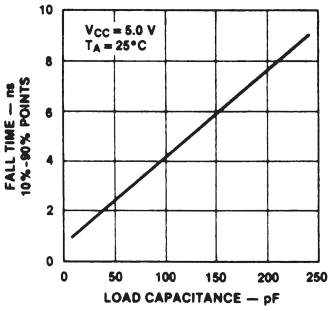

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Figure 6. Fall Time VS Load Capacitance

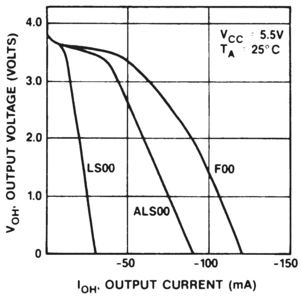


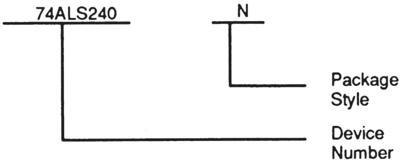
Figure 7. Output HIGH Characteristics

Ordering Information

Signetics commercial ALS products are generally available in both standard dual–in–line and surface mounted options. The ordering code specifies temperature range, device number, and package style as shown below. For commercial products, the standard temperature range is 0–70°C. Available package options are shown on individual data sheets in the "Ordering Information Table". For surface mounted devices, the SO plastic dual–in–line package is supplied up to and including 28 pins. Above 28 pins, the plastic leaded chip carrier is utilized.

A wide variety of functions and package options is available for military products. Information on military products is available from the nearest Signetics sales office, sales representative, or authorized distributor. The Signetics Military Products Data Manual contains specifications, Package, and Ordering Information for all military–grade products.

ORDERING CODE EXAMPLES



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
Commercial Range 0°C to 70°C	74ALSXXX	N = Plastic DIP D = Plastic SO DIP (surface mounted) A = Plastic Leaded Chip Carrier
Military Range –55°C to 125°C	See Military Products Data Manual	

Section 1
Function Selection Guide

Function Selection Guide

GATES

FUNCTION	DEVICE NUMBER	PINS
INVERTERS Hex Inverters	74ALS04B	14
NAND Quad 2–Input Triple 3–Input Dual 4–Input 8–Input Quad 2–Input NAND, OC	74ALS00A 74ALS10A 74ALS20A 74ALS20A 74ALS38A	14 14 14 14
NOR Quad 2–Input Triple 3–Input	74ALS02 74ALS27	14 14
AND Quad 2–Input Triple 3–Input	74ALS08 74ALS11A	14 14
OR Quad 2–Input	74ALS32	14
EXCLUSIVE–OR Quad 2–Input	74ALS86	14

FLIP–FLOP

FUNCTION	DEVICE NUMBER	PINS	CLOCK EDGE	INV	NINV
D	74ALS74A	14	↑	X	X
JK	74ALS109A	16	↑	X	X
JK	74ALS112A	16	↓	X	X
Quad D	74ALS175	16	↑	X	X
Hex D	74ALS174	16	↑		X
Octal D	74ALS273	20	↑		X
Octal D, with Enable	74ALS377	20	↑		X
Octal D, 3–State	74ALS374	20	↑		X
Octal D, 3–State	74ALS564A	20	↑	X	
Octal D, 3–State	74ALS574A	20	↑		X

Function Selection Guide

LATCHES

FUNCTION	DEVICE NUMBER	PINS	NINV	INV	3–STATE
Octal	74ALS373	20	X		X
8–Bit Transparent	74ALS563A	20		X	X
8–Bit Transparent	74ALS573B	20	X		X

MULTIPLEXERS/ENCODERS

FUNCTION	DEVICE NUMBER	PINS	NINV	INV	3–STATE
Dual 4–Input	74ALS153	16	X		
Dual 4–Input	74ALS253	16	X		
Quad 2–Input	74ALS157	14	X		
Quad 2–Input	74ALS158	14		X	
Quad 2–Input	74ALS257	16	X		X
Quad 2–Input	74ALS258	16		X	X
8–Input	74ALS151	16	X	X	
8–Input	74ALS251	16	X	X	X

DEMULTIPLEXERS/DECODERS

FUNCTION	DEVICE NUMBER	PINS
Dual 1–of–4	74ALS139	16
1–of–8	74ALS138	16

BUFFERS

FUNCTION	DEVICE NUMBER	PINS	NINV/INV	3–STATE OPEN COLLECTOR
Octal Buffer	74ALS240A/240A–1	20	INV	3–State
Octal Buffer	74ALS241A/241A–1	20	NINV	3–State
Octal Buffer	74ALS244A/244A–1	20	NINV	3–State

SHIFT REGISTERS

BITS	SERIAL IN	PARALLEL IN	SERIAL OUT	PARALLEL OUT	DEVICE NUMBER	CLOCK EDGE
8	X			X	74ALS164	↑

Function Selection Guide

COUNTERS

FUNCTION	DEVICE NUMBER	PINS	TYPE	PRESETTA-BLE	PARALLEL ENTRY	CLOCK EDGE
Synchronous	74ALS161B	16	BCD	X	S	↑
Synchronous	74ALS163B	16	BCD	X	S	↑
Up/Down	74ALS191	16	BCD	X	A	↑
Up/Down	74ALS193	16	BCD	X	A	↑

TRANSCEIVERS

FUNCTION	DEVICE NUMBER	PINS	NINV/INV	3–STATE OPEN COLLECTOR
Octal Transceiver	74ALS245A/245A–1	20	NINV	3–State
Octal Transceiver	74ALS645A/645A–1	20	NINV	3–State
Octal Transceiver	74ALS620A/620A–1	20	INV	3–State
Octal Transceiver	74ALS623A/623–1	20	NINV	3–State
Octal Latched Transceiver	74ALS543/543–1	24	NINV	3–State
Octal Latched Transceiver	74ALS544/544–1	24	INV	3–State
Octal Transceiver/Register	74ALS646/646–1	24	NINV	3–Sate
Octal Transceiver/Register	74ALS648/648–1	24	INV	3–State
Octal Transceiver/Register	74ALS651/651–1	24	INV	3–State
Octal Transceiver/Register	74ALS652/652–1	24	NINV	3–State

Section 2
Quality And Reliability

Quality And Reliability

SIGNETICS' QUALITY PROGRAM

In 1979, Signetics recognized that quality was becoming a major competitive issue, not only in the semiconductor business, but also in other industries. Increases in the volume of products imported from the Far East (steel, automobiles, and consumer electronics) sent strong signals that new competitive forces were at work.

Signetics quickly began to investigate a variety of quality programs. The company realized that quality improvement would require a contribution from all employees. Management commitment and participation, however, was recognized as the primary prerequisite for this program to work successfully. Resources required for the resolution of defects were under management control.

In 1980, Signetics developed a program which focused on quality management. Rearranging previous quality control philosophies, Signetics developed a decentralized, distributed quality organization and simultaneously installed a quality improvement process based on the 14-Step improvement program advocated by Phil Crosby. The process was formally begun company-wide in 1981.

Since then, substantial progress has been made in every aspect of Signetics' operations. From incoming raw material conformance to improvements in administrative clerical errors -- every department and individual is involved and striving for Zero Defects. Zero Accept sampling plans and Zero Defects warranties are evidence of Signetics' ongoing commitment and progress in quality.

Today, Signetics' quality improvement process has had a far-reaching impact on all aspects of our business. Signetics provides its customers with products of refined electrical and mechanical quality. And through continual use and modification of the Crosby program, Signetics is providing itself with a well-defined method of managing ongoing improvement efforts.

SIGNETICS' ZERO DEFECTS WARRANTY

In recent years, American industry has demanded increased product quality of its IC suppliers in order to meet growing international competitive pressure. As a result of this quality focus, it is becoming clear that what was once thought to be unattainable -- Zero Defects -- is, in fact, achievable.

Signetics offers a Zero Defects Warranty which states that it will take back an entire lot if a single defective part is found. This precedent setting warranty has effectively ended the IC industry's "war of the AQLs" (Acceptable Quality Levels). The ongoing efforts of IC suppliers to reduce PPM (Parts Per Million) defect levels is now a competitive customer service measure.

This intense commitment to quality provides an advantage to today's electronics OEM. That advantage can be summed up in four words: ***Reduced Cost of Ownership***

As IC customers look beyond purchase price to the total cost of doing business with a vendor, it is apparent that a quality-conscious supplier, like Signetics, represents a viable cost reduction resource. Consistent high-quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures

SIGNETICS' STATISTICAL PROCESS CONTROL (SPC)

Although application of statistics in our process development and manufacturing activities goes back to the early 1970's, the corporate-wide emphasis on Statistical Process Control (SPC) did not come about until mid-1984.

Prior to 1984, 14 full-time statisticians were active in statistical training, problem solving, general consulting, and designing experiments. However, 1984 shifted the emphasis from a sporadic and uncoordinated effort to a corporate-wide coordinated and disciplined approach to SPC.

This shift in emphasis came about for two main reasons:

Customers' realization of importance and relevance of SPC to quality and reliability issues.

A natural evolution of our four year old quality process made introduction of SPC and other related programs an inevitable event. SPC was, therefore, introduced under the quality umbrella.

The objective of the SPC program is to introduce a systematic and scientific approach to business and manufacturing activities. This approach utilizes sound statistical theory. Managers are expected to be able to turn data into information, and make decisions solely based on data (not perceptions).

The most critical and challenging aspect of implementing SPC is establishment of a discipline within the operating areas so that decision making is fundamentally based on verifiable data, and actions are documented. The other is realization of the fact that statistical tools merely point out the problems and are not solutions by themselves. The burden of action on the process is still on the implementers' shoulders. In order to implement SPC effectively, three steps are continually followed:

Documenting and understanding the process, using process flow charts and component diagrams.

Establishing data collection systems, and using SPC tools to identify process problems and opportunities for improvement.

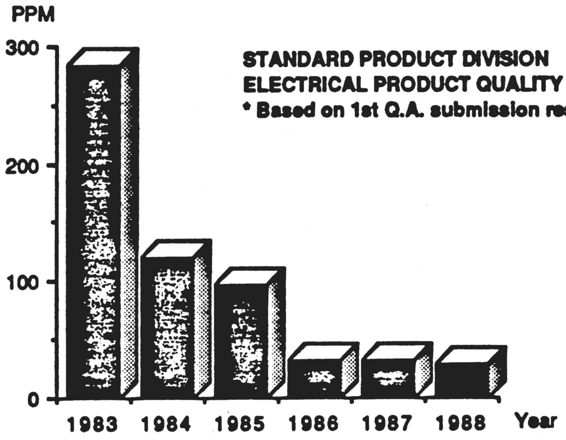
Acting on the process, and establishing guidelines to monitor and maintain process control.

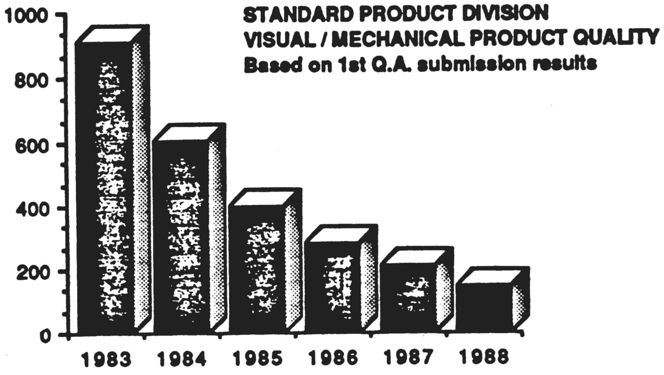
Repeating steps 1-3 again.

These fundamentals are the basis of establishing Signetics' specifications and operating philosophy with respect to SPC. Signetics believes a solid foundation creates a permanent system and accelerates our quality improvement process.

SIGNETICS QUALITY PERFORMANCE

Signetics Quality Improvement Program has influenced our entire production cycle -- from the purchase of raw materials to the shipment of finished product. The involvement of all areas of the company has resulted in impressive quality improvements. A traditional quality gauge is final product electrical and visual-mechanical defect levels as measured upon first submittal results at Signetics outgoing Quality Assurance gates (Figures I and II). Current product shipments routinely record below 20 PPM (Parts Per Million) electrical defect levels and 150 PPM visual-mechanical defect levels. Since Signetics utilizes zero accept sampling on all finished product inspection, any lot with one or more rejects is 100 percent re-tested .





The most meaningful measure of our product quality is how we measure up to our customers' expectations. Many customers routinely send us incoming inspection data on our products. One major mainframe manufacturer has reported zero defects in electrical, visual-mechanical, and hermeticity and has reported a 100 percent lot acceptance rate on Signetics' Standard Products products for over a year. Due to this type of performance, an increasing number of our customers are eliminating expensive incoming inspection testing and have begun implementation of Signetics' Ship-to-Stock program.

SIGNETICS' SHIP-TO-STOCK PROGRAM

Ship-to-Stock is a formal program developed at the request of our customers to help them reduce their costs by eliminating incoming test and inspection. Through close work with these customers in our quality improvement program, they became confident that our defect rates were so low that the redundancy of incoming inspections and testing was not only expensive, but unnecessary. They also saw that added component handling increased the potential of causing defects.

Ship-to-Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into the customer's assembly line or inventory. This program was developed at the request of several major manufacturers after they had worked with us and had a chance to experience the data exchange and joint corrective action occurring as part of our quality improvement program.

Manufacturers using large volumes of ICs, those who are evaluating Just-in-Time delivery programs, or those who want to reduce or avoid high-cost incoming inspection are strongly encouraged to participate in this worthwhile program. Contact your local Signetics' sales representative for further assistance and information on how to participate in this program.

SUMMARY

The Signetics Quality Improvement Program has had a far-reaching impact on all aspects of our business. It has, of course, provided our customers with products of improved electrical and mechanical quality and has provided Signetics with a method of managing product reliability improvement to ensure that Signetics' products continue to perform as specified.

The corrective action teams that work to eliminate the cause of defects in Signetics' products are committed to producing highly reliable integrated circuits and, as demonstrated by our continually improved product reliability performance, we are well on the way to achieving our objective, ZERO DEFECTS.

RELIABILITY ASSURANCE PROGRAMS

FOCUS ON PRODUCT RELIABILITY

During the period from 1981 to 1984, continuing improvements in process and material quality had a significant impact on product reliability.

Since 1984, Signetics has intensified its efforts to markedly improve product reliability. Corporate Reliability Engineering, Division and Plant Reliability Units, Philips Research Labs-Sunnyvale, and Manufacturing Engineering work jointly on numerous improvement activities. These focused activities enhance the reliability of Signetics future products by providing improved methods for reliability assessment, increased understanding of failure physics, advanced analytical techniques, and aid in the development of materials and processes.

RELIABILITY MEASUREMENT PROGRAMS

Signetics has developed comprehensive product and process qualification programs to assure that its customers are receiving highly reliable products for their critical applications. Additionally, ongoing reliability monitoring programs, SURE III and Product Monitor, sample standard production product on a regularly established basis (see Table I below).

Table I
Reliability Assurance Programs

Reliability Function	Typical Stress	Frequency
New Process Qualification	High Temperature Operating Life Biased Temperature-Humidity, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each new wafer fab process
New Product Qualification	High Temperature Operating Life Biased Temperature-Humidity, Static High Temperature Storage Life Pressure Pot Temperature Cycle Electrostatic Discharge Characterization	Each new product
SURE III	High Temperature Operating Life Biased Temperature-Humidity, Static High Temperature Storage Life Pressure Pot Temperature Cycle Thermal Shock	Each fab process family, every four weeks
Product Monitor	Pressure Pot Thermal Shock	Each package type and technology family at each assembly plant, every week

DESCRIPTION OF STRESSES

SHTL -- Static High Temperature Life: SHTL stressing applies static DC bias to the device. This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive contaminants to the silicon surface. The voltage bias must be maintained until the devices are cooled down to room temperature from the elevated life test temperature. DHTL stressing is not as effective in detecting such problems because the bias continuously changes, intermittently generating and healing the problem. For this reason, SHTL has typically been used as the accelerated life stress for Standard Products products.

HTSL -- High Temperature Storage Life: This stress exposes the parts to elevated temperatures (150ºC-175ºC) with no applied bias. For plastic packages, 175ºC is the high end of its safe temperature region without accelerating untypical failure mechanisms. This test is intended to accelerate mechanical package-related failure mechanisms such as Gold-Aluminum bond integrity and other process instabilities.

THBS -- Biased Temperature-Humidity, Static: This accelerated temperature and humidity bias stress is performed at 85ºC and 85% relative humidity (85ºC/85% RH). In general, the worst case bias condition is the one which minimizes the device power dissipation and maximizes the applied voltage. Higher power dissipations tend to lower the humidity level at the chip surface and lessen the corrosion susceptibility.

TMCL -- Temperature Cycling, Air-to-Air: The device is cycled between the specified upper and lower temperature without power in an air or nitrogen environment. Normal temperature extremes are -65ºC and +150ºC with a minimum 10 minute dwell and 5 minute transition per Mil-STD-883C, Method 1010.5, Condition C. This is a good test to measure the overall package to die mechanical compatibility, because the thermal expansion coefficients of the plastic are normally very much higher than those of the die and leadframe. However, for large die the stress may be too severe and induce failures that would not be expected in a real application.

PPOT -- Pressure Pot: This stress exposes the devices to saturated steam at elevated temperature and pressure. The standard condition is 20 PSIG which occurs at a temperature of 127ºC and 100% RH. The stress is used to test the moisture resistance of plastic encapsulated devices. The plastic encapsulant is not a moisture barrier and will saturate with moisture within 72 hours. Since the chip is not powered up the chip temperature and relative humidity will be the same as the autoclave once equilibrium is reached. Because the steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, it is effective at detecting corrosion problems, contamination induced leakage problems, and general glassivation stability and integrity. It is also a good test for both package integrity (cracks in the package), and for die cracks (the moisture swells the plastic enough to stress the die -- also the moisture causes leakage paths in the crack itself).

TMSK -- Thermal Shock, Liquid-to-Liquid: Similar to TMCL, however, heating and cooling are done by immersing the units in hot and cold inert liquid. Temperature extremes are -65ºC to +150ºC with a minimum 5 minute dwell and less than 10 second transition per Mil-STD-883C, Method 1011.4, Condition C. Since heat transfer by conduction is generally much faster than by convection, the liquid-based thermal shock causes more rapid temperature changes in the part. Also, as the part is rapidly changing in temperature all its mass will not be in equilibrium and the temperature gradients across the part will produce additional mechanical stress. For chip-out under bond these factors combine to give an acceleration of 1.5X over TMCL. For ball neck break (wire creep) failures, acceleration of 10X has been observed. To date, there is no reasonable explanation for why the relative accelerations in TMCL and TMSK are so variable and dependent on the failure mechanism.

PRODUCT AND PROCESS QUALIFICATIONS

Qualification activity is centered around new products and processes and changes in products and processes. The goal is to assure that the products can meet the qualification requirements prior to general release, and on an ongoing basis to demonstrate conformance to those requirements. The nature and extent of reliability stressing required depends on the type of change and the amount of applicable reliability data available.

A full qualification may include Early Failure Rate (EFR), Intrinsic Failure Rate (IFR), and Environmental Endurance Stressing. Such stress plans are reserved for introductions or changes that involve new or untested material or processes and, as such should be subjected to the maximum reliability interrogation. This normally entails a full range of biased and unbiased temperature and humidity stresses along with thermo-mechanical stresses.

For changes that are of limited scope, the full range of qualification stressing may not be warranted. In these instances, the nature and extent of the change is examined and only those stresses which provide a valuable measure of the change, or those which will detect potential weaknesses, are performed.

SIGNETICS' SELF-QUAL PROGRAM (SSQP)

Self-Qual is a joint program between Signetics and a customer which formally communicates Signetics' qualification activities for a new or changed product, process, or material. The Signetics Self-Qual process provides our customer's engineering groups an opportunity to participate in the development of the qualification plan. During the qualification process, customers may audit the project, and can receive interim updates of qualification progress. Upon completion, formal detailed engineering reports are provided.

The major impact to the customer comes from the reduced workload on the component engineering and qualification groups. These engineering resources generally divide their time between routine qualification activity and problem resolution on critical components. By eliminating the need to perform qualification for some of the basic vendor changes the customer component engineer can spend more of his time resolving the critical product issues. In addition, the total amount of stress hardware needed to perform qualification life tests and other environmental evaluations can be reduced, saving the customer facility costs and reducing operating expense.

Self-Qual is a no-risk proposition for the customer. Each Self-Qual proposal provides a detailed description of what we are changing and why. It includes a detailed plan of what we intend to do to establish the reliability of the products affected. If the customer wishes to have products added to the plan, or select some additional stresses, or prefers alternative stress conditions, Signetics will do everything possible to accommodate those requests. After that, if the customer is still uncomfortable with the recommended change, they are under no obligation to accept our data, and they may perform their own qualification program in addition to Signetics.

Customers who are interested in participating in this program should contact their local Signetics sales representative or Signetics' Corporate Reliability Engineering department directly.

SURE III RELIABILITY MONITORING PROGRAM

In order to implement an improvement program, a standard measure of performance was needed. Signetics uses the results from the SURE III Reliability Monitoring Program as its basic ongoing measure of product reliability performance. This program samples all generic families of products manufactured by Signetics, and utilizes standardized stress methods and test procedures. This system is augmented by new product and process qualification activities and infant mortality monitoring programs.

Signetics adopted a measurement philosophy based on the premise of continual improvement toward our performance standard of zero defects.

We also increased our standard Pressure Pot stress conditions from 15 PSIG/121°C to 20 PSIG/127°C. This reduced stress duration from 168 hours to 72 hours, and increased high volume sampling, which increased sensitivity to low defect levels.

Our standard monitoring program, SURE III, includes the following stress conditions:

High Temperature Operating Life: (SHTL)	Tj ≥ 150°C, Ta = 125°C to 150°C, Bias condition = Static, Vcc = MAX*, Duration = 1000 Hours
High Temperature Storage Life: (HTSL)	Ta = 150°C, No Bias, Duration = 1000 Hours
Static Biased Temperature-Humidity: (THBS)	Temperature = 85°C ± 3°C, Humidity = 85% RH ± 5%, Bias condition = Static, Vcc = MAX*, Duration = 1000 Hours
Temperature Cycle: (TMCL)	Condition = Air-to-Air -65°C (+0°C -10°C) to +150°C (+10°C -0°C), Dwell = 10 minutes minimum each extreme, No bias, Duration = 1000 Cycles (plastic); Cycles (hermetic)
Pressure Pot:	Condition = 127°C (+2°C -2°C), 20 PSIG (+0.5 -0.5 PSIG), (PPOT) 100% saturated steam, No bias, Duration = 72 Hours
Thermal Shock: (TMSK)	Condition = Liquid-to-Liquid -65°C (+0°C -10°C) to 150°C (+10°C -0°C), Dwell = 5 minutes minimum each extreme, No bias

NOTE:

* Vcc MAX is generally = Data Book Maximum Specified Vcc.

PRODUCT MONITOR

In addition to the SURE III program, each Signetics assembly plant performs Pressure Pot (20 PSIG, 127°C, 72 Hours) and Thermal Shock (-65°C to +150°C, 300 Cycles) reliability monitors on a weekly basis for each molded package type by pin count. The purpose of this program is to monitor the consistency of the assembly operations for such attributes as molding quality and die attach and wire bond integrity. These data are reported back to manufacturing operations and corporate and divisional reliability and quality assurance departments by electronic mail each week. The data from the weekly product monitor is summarized along with the SURE III program reliability data in this publication.

RELIABILITY EVALUATIONS

In addition to the product performance monitors encompassed in the SURE III program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities, and subcontractors.

Device or generic group failure rate studies.

Advanced environmental stress development.

Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE III program, however, more highly-accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are often included in some evaluation programs.

STRESS FACILITY QUALITY

Signetics quality improvement has reached all functional areas of the company, and the reliability stress laboratories are no exception. Corporate Reliability Laboratory (CRL) is one of the many areas where the benefits of the quality improvement process pays repeated dividends.

CRL utilizes stresses which accelerate failure rates hundreds to thousands of times, requiring precision and control to make reliability data meaningful. Stress loading schedules are maintained with absolute regularity and chambers are never off-line beyond scheduled loading plans. Board currents are recorded prior to and at each interval on biased stresses, and monitoring of in-oven currents is conducted daily.

Thermal modeling of both Thermal Shock and Temperature Cycling systems has been accomplished and all loads are carefully weighed to ensure that thermal ramps are consistent.

Pressure Pot and Biased Pressure Pot systems utilize microprocessor controllers, and are accurate to within 0.1 degree centigrade. Saturation is guaranteed via automatic timing circuits, and a host of fail-safe controls ensure that test groups are never damaged.

Electrostatic discharge (ESD) handling precautions are standard procedures in the laboratories, and the occurrences of devices lost, zapped, or overstressed have become almost non-existent.

RELIABILITY IMPROVEMENT PROGRAMS

Currently, Signetics is involved in a number of reliability improvement programs intended to enhance product reliability performance. A series of activities are currently addressing failure rate reduction in thermal cycling stresses, particularly on large die. Other reliability improvement programs involve the use of Silicon Nitride and other technologically advanced passivation systems to increase the high humidity resistance of sensitive products.

Reducing early life failures has become a major focus at Signetics. Numerous corrective action teams are in the process of establishing high volume monitors capable of accurately describing parts per million (PPM) level infant failure rates. From data produced via these monitors, improvement in wafer fabrication process and assembly process technologies are developed to minimize integrated circuit defect levels.

RELIABILITY PUBLICATIONS

Data from all of these activities is made available to all Signetics customers in a variety of publications:

PRODUCT RELIABILITY SUMMARIES and QUARTERLY UPDATES

Yearly, each Product Division's SURE III monitoring data is summarized and published in a Product Reliability Summary. Quarterly, an update is published for the data accumulated during interim periods.

SSQP - SIGNETICS SELF-QUAL PROGRAM

In addition to the regular publications of reliability monitor results, a special program for the publication of qualification proposals and final engineering reports has been in place since January of 1984.

SMD RELIABILITY

In support of Signetics' leadership in Surface Mount Device (SMD) technology, we have published indepth studies and evaluations on the reliability of numerous combinations of SMD packages and IC process technologies. These reports cover not only the basic product performance, but also evaluate products after exposure to the unique environments created by the various SMD soldering and cleaning processes.

SPECIAL RELIABILITY REPORTS

In addition to our standard reports, special reliability evaluation results are available on a wide variety of Signetics' products and processes. Custom reports can be generated to meet specific customer needs and the most accurate failure rate estimates can be prepared for your specific system application and environment.

DATA AVAILABILITY

The previously referenced documents are available to all Signetics customers. Many are available in your local Signetics sales office, or:

Corporate Reliability Services
Reliability Publications Group
Department 9605, Mail Stop #34
Arques Avenue
Box 3409
Sunnyvale, CA 94088-3409

where you can be placed on a standard mailing list for all documentation which meet your specific requirement(s).

SIGNETICS' MANUFACTURING FACILITIES

Signetics, as part of a multinational corporation, utilizes manufacturing facilities for wafer fabrication, package assembly, and test in three states and three overseas countries as shown in Table XII. All wafer fabrication is performed in Signetics operated fabs which report to the Vice President of Die Manufacturing Operations (DMO) in Sunnyvale. Similarly, Signetics Assembly operations in Utah, Korea, and Thailand, report to the Vice President of Assembly Manufacturing Operations (AMO). Assembly subcontractors, Pebei and Anam, are scheduled and controlled through the AMO organization. Assembly subcontractors process all product to Signetics' specifications and materials. Signetics has on-site quality assurance personnel at each subcontractor to audit assembly processes and procedures.

All Signetics products are electrically tested in Signetics operated facilities. These facilities report to the manufacturing organization (DMO or AMO) operating the facility at which they are located.

Table V
Signetics' Product Manufacturing Facilities

WAFER FABRICATION FACILITIES

Designation	Location	Process Families
Fab 01	Sunnyvale, California	Bipolar Junction Isolated
Fab 09	Orem, Utah	Bipolar Gold Doped
Fab 16	Sunnyvale, California	Oxide Isolated
Fab 21	Orem, Utah	Bipolar Schottky
Fab 22	Albuquerque, New Mexico	ACMOS

ASSEMBLY FACILITIES

Designation	Location	Package
SigKor	Seoul, Korea	DIP, SO, and PLCC
SigThai	Bangkok, Thailand	DIP and CERDIP
Orem	Orem, Utah	Military "Jan" Hermetic
Pebei	Kaomsiung, Taiwan	SO
Anam	Seoul, Korea	SO and Metal Can

TEST FACILITIES

Designation	Location	Package
TA03	Sunnyvale, California	Wafer Sort, Final Test and Quality Assurance
SigKor	Seoul, Korea	Final Test and Quality Assurance
SigThai	Bangkok, Thailand	Final Test and Quality Assurance
Sacto	Sacramento, California	Military Final Test and Quality Assurance

TYPICAL IC MANUFACTURING FLOW

The manufacturing process for Integrated Circuits begins with wafer fabrication. The wafers are then electrically sorted, assembled, and tested prior to customer shipment. Quality assurance inspections are utilized throughout the manufacturing process. Table VI contains a typical manufacturing flow for Signetics' ICs.

Table VI

Typical I.C. Manufacturing Flow
For Bipolar Junction Isolated Product

Wafer Fab:	Initial Oxidation
	Buried Layer Diffusion
	Epitaxial Layer
	Isolation Diffusion
	Base Diffusion
	Emitter Diffusion
	Contact Mask
	Metallization #1
	Dielectric Glass Layer
	Metallization #2
	Nitride Passivation
Wafer Sort:	Wafer Electrical Test
	Wafer Visual Acceptance
Assembly:	Saw Scribe and Break
	Die Sort Visual Acceptance
	Die Attach to Leadframe
	Wire Bonding
	Pre-Seal Visual Acceptance
	Encapsulation
	Topside Symbolization
	Leadframe Trim and Form
	Solder Coat
	Mechanical/Visual Acceptance
Test:	Final Electrical Test
	Burn-In (Optional)
	Product Assurance Test
Shipping:	Pack-Out
	Outgoing Quality Control Acceptance
	Shipping

Package Construction

	PDIP	SO/PLCC	CERDIP
Lead Frame	Copper, 194 Alloy	Copper, 194 or PMC102	Alloy-42
Lead Finish	Tin/Lead Solder Dip or Tin/Lead	Tin/Lead Solder Dip (60/40) Solder Plate (80/20)	Tin/Lead Solder Dip
Bond Area Finish	Silver Spot	Silver Spot	Silver Spot
Die Attach	Silver Filled Polyimide or Thermoplastic	Silver Filled Polyimide or Thermoplastic	Silver Filled Glass
Bond Wire	Gold, 1.0-1.3 mil. Diameter	Gold, 1.0-1.3 mil. Diameter	Aluminum, 1.0 mil. Diameter
Wire Bonding	Thermosonic	Thermosonic	Ultrasonic
Die	Ball	Ball	Stitch
Leadframe	Stitch	Stitch	Stitch
Package Material	Novolac Epoxy	Novolac Epoxy	Ceramic

Package Code Definitions

Pin Count	PDIP	SO	PLCC	CERDIP
NE	DE	----	FE	
NH	DH	----	FH	
NJ	DJ	----	FJ	
NK	----	----	FK	
NL	DL	AL	FL	
NM	----	----	FM	
NN	DN	----	FN	
NQ	----	AQ	FQ	
----	----	AA	----	

Section 3
Circuit Characteristics

Circuit Characteristics

INPUT STRUCTURES

There are two types of input structures used in ALS circuits: diffusion diode and PNP vertical transistor. Each of these are discussed below.

The diffusion diode input is used occasionally with ALS circuits. The input diode is labeled as D1 in Figure 1. There can be more than one if NAND logic is to be performed. In the oxide-isolated processes these are base-collector diffusions. Each input pin also has a Schottky clamp diode D2. This diode is standard for most TTL circuits, and is included to limit negative input voltage excursions that are generally the result of inductive undershoot.

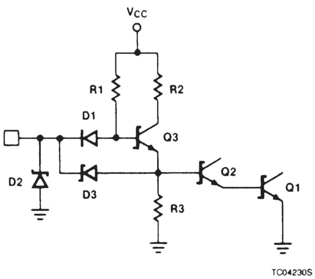


Figure 1. Diode Input

The static diode input function of voltage versus current is shown in Figure 2. If the pin voltage is negative, most of the relatively high negative current flows through the clamp Schottky D2. At 0V the current flows from V_{CC} through R1 and D1 to the pin. Switching from a logic Low level to a logic High level occurs when the input pin voltage rises high enough to force the current from the D1 path to the Q3 - Q2 - Q1 path. This happens when the base voltage of transistor Q3 is at three base-emitter drops ($3V_{BE}$), and the pin is at $2V_{BE}$, which is the standard ALS threshold switching voltage. At this voltage the input current is very small, just the leakage currents of diodes D1, D3, and clamp diode D2. The current remains at this small, positive value until breakdown voltage is reached.

Transistor Q3 and resistor R2 provide a current gain by increasing the amount of current available to Q2 and Q1 when the pin voltage is high. R3 bleeds current off the base of Q2 to pull it low when the pin voltage is low. D3 speeds up this process during the High-to-Low pin transition. When the switching transients are over, D3 is reverse biased.

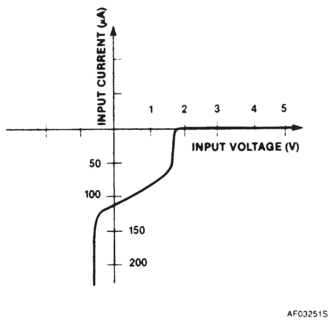


Figure 2. Static Diode Input Function of Voltage VS Current

The current of Figure 2 is scaled for the case where the pin is required to pull down a single 40KΩ resistor R1 (20µA maximum in the High state and 0.2mA maximum in the Low state). For some parts, pin current can be higher, especially in the logic Low state. This increase will happen if the pin must sink the current from more than one R1 resistor, or if the value of R1 is less than 40KΩ, which will be the case if the capacitance at the base of the transistor Q3 is too large for the required switching speed.

The PNP vertical transistor has found wide acceptance in its various forms in low power Schottky logic because it provides a high-impedance input which is usually desirable. It is now frequently the input of choice for new parts built with improved processes. The PNP transistor Q3 is fabricated with the P-type substrate as the grounded collector, the N-type Epi as the base, and the P-type normal base diffusion as the emitter. The process must be tailored to provide a suitable current gain for this vertical structure and must have provision to remove the considerable substrate current without an appreciable rise in substrate voltage. Referring to Figure 3, Q3 functions as an emitter follower for pin voltages low enough to provide an emitter-base forward bias. This occurs at an emitter voltage below the $3V_{BE}$ value provided by the D3 - Q2 - Q1 stack, and gives the desired $2V_{BE}$ pin threshold. At pin voltages above this value, Q3 turns off and the current through R1 is directed to Q2 - Q1 through D3. The Schottky diode D2 speeds up the High to Low transition if the pin voltage falls more rapidly than the base of Q2; otherwise, D2 is off. The PNP input characteristics are shown in Figure 4. If the input voltage is negative with respect to ground, a large clamp current flows through D_1. As the voltage rises, D_1 turns off and the input current falls to the base current of Q3; for the usual values of R_1, this is in the range of about 3µA. This decreases as the lead voltage rises. At threshold, Q3 turns off and the input current drops to a low value determined by the leakage of D_1, D_2, and Q3. The current remains at this low value until the onset of breakdown. Since all PNP inputs are protected with ESD structures, the breakdown current is set by this, and not the actual PNP device.

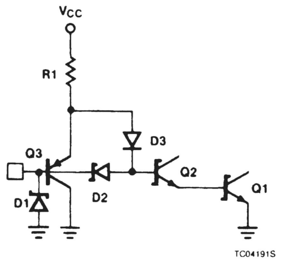


Figure 3. PNP Input

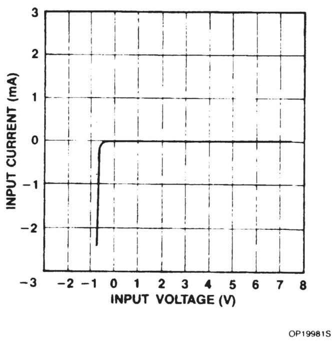


Figure 4. PNP Input Characteristics

INPUT CONSIDERATIONS

Static Input Current

A comparison of input current for various input voltage ranges for both types of inputs is shown in Figure 8.

Diode inputs supply current to their drivers that may be as large as 200μA at V_{IN} of 0.5V for a single unit load input. Signetics ALS parts are designed to have input current less than 20μA over the full switching range from 0V to V_{CC}. Typical PNP input current is less than 10μA below threshold voltage and 1μA above threshold.

INPUT VOLTAGE RANGE	INPUT CURRENT	
	Diode	PNP
Below Ground	Schottky Clamp	Schottky Clamp
Ground to V_T	High (to 200μA)	Low (to 20μA)
V_T to V_{CC}	Leakage	Leakage
Above V_{CC}	Leakage	Leakage

Figure 5. Input Current for Input Voltage Ranges

Input Capacitance

Input capacitance, measured using a small-signal variation about a static DC operating point, is low for ALS inputs. When one includes the added capacitance of the elements common to each input, such as the pin, pad, bond wire, and clamp Schottky diode, the percentage difference for total static input capacitance for either type of input is not very large.

Dynamic Input Current

In many applications the total current an input pin draws during a switching transition is a more important consideration than its input capacitance. This dynamic input current is often larger than the value of static capacitance would predict because both types of input structures normally include some sort of speed-up mechanism, usually a "kicker" Schottky diode, connected to an internal node of the circuit. The kickers deliver current, related in a non-linear way to input edge-rates. High-dynamic input current does not always equate to fast circuit switching. The percentage differences for dynamic current tend to be larger than the respective differences for static capacitance.

Switching Threshold Voltage

The ALS input switching threshold voltage is set quite high for TTL at two base-emitter junction forward-bias drops. ALS input structures have enough gain that the voltage range in which they switch from one state to the other, as shown by a static DC transfer function curve, is completed within about 100mV of the $2V_{BE}$ threshold. For a typical part at room temperature, V_{BE} is about 800mV, and the switching threshold is nominally at 1.6V; the static transfer range uncertainty of about 100mV gives a nominal threshold for solid Lows and Highs of about 1.55V and 1.65V respectively. The ALS threshold voltage was chosen higher than other TTL families to give a larger noise margin with respect to ground, and to be more nearly centered in the region where a ALS output driver stage switches with maximum edge rates, which occurs between about 0.6V and 2.6V.

Because the ALS threshold is set by the base-emitter junction voltage, it is dependent on junction temperature and current density. V_{BE} increases by about 1.2mV for each degree C drop in junction temperature; current density changes by about a decade for a 60mV change in V_{BE}. The total variation due to processing differences, temperature, and current density is about 150mV per junction, or 300mV total change in input threshold to give limits of 1.25V Low and 1.95V High. The ALS V_{IL} and V_{IH} limits are 0.8V and 2.0V respectively, a tight spec for V_{IH}.

ELECTRO-STATIC DISCHARGE (ESD) CONSIDERATIONS

It is universally true that no bipolar integrated circuit process can provide devices with such high breakdown voltages that they are able to withstand any level of ESD without some structure punching through or breaking down. The necessary condition for survival when this occurs is that the energy dissipation in any volume of the chip must be kept low enough so that neither the silicon nor the interconnecting metal can melt. This can be accomplished in two ways: the breakdown voltage should be as low as practical, consistent with normal circuit operation, and the energy should be dissipated in as large a volume as is possible. Circuit components that are particularly sensitive to charge damage must be protected by structures that are less fragile. All Signetics ALS parts are designed with these requirements in mind, and although, as a rule of thumb, a sophisticated oxide isolated process used to fabricate these parts tends to be more ESD damage-prone than a junction isolated process, ALS is as rugged as other TTL families in general. If ALS parts are handled with the same care afforded any other high-technology parts, they will not be damaged.

ESD sources usually fit into one of two categories: people or other objects that have accumulated static charge and touch the parts; or, they generate their own charge, as is the case when a circuit makes sliding contact with an insulator. In the first instance, static voltages tend to be high, over 10000V, and discharge is usually limited by relatively high series resistance. In the second case, voltages are lower, around 200V, but there is very little series resistance to limit discharge current. Both possibilities are simulated with discharge models that are used in the majority of the test setups, and parts are designed in a way to improve survival for both ESD conditions.

Experience has shown that inputs of TTL circuits are much more likely to suffer ESD damage than outputs. Since negative voltages are discharged through clamp ground diodes with low chip dissipation, only voltages positive with respect to substrate ground are apt to produce input damage.

PNP and diode inputs have a positive voltage breakdown in the relatively high range of from 15V to 25V. Schottky diodes connected to an input pin usually break down before junction diodes, and if they are stressed beyond their limits the Schottky diodes usually sustain damage in the corners. A diffusion guard-ring around the diode increases the uniformity of the breakdown, and as a result maximizes the dissipation volume at breakdown and increases the ability of the device to survive ESD. All Signetics ALS circuits have guard-rings on Schottky diodes that connect to input or output pins.

Signetics ALS parts also have specific ESD structures included which protect up to 2000V for the standard resistance limited case — the human body model.

FLOATING INPUTS

ALS inputs should not be allowed to float. All unused inputs, even those on unused gates, should be tied to a voltage source of relatively low impedance that will get them out of the logic picture and out of trouble. For a Low input this can be ground, or the output of a permanently low driver. For a High input this can be V_{CC}, protected by a series resistor if circuit damaging voltage spikes are possible in the system, or a permanently high driver.

Properly tied High or Low inputs will not pick up enough spurious noise to cause problems. If they are allowed to float, the results can be disastrous. Floating diode inputs usually pull to within a few mv of $3V_{BE}$ above ground, a V_{BE} above threshold. The input voltage will fall about 1V per 0.1mA of current that is capacitively coupled from an adjacent Low-going pin. Since pin-to-pin input capacitance is in the order of one pF for an IC in a PC environment, an adjacent pin falling at 1.0V/

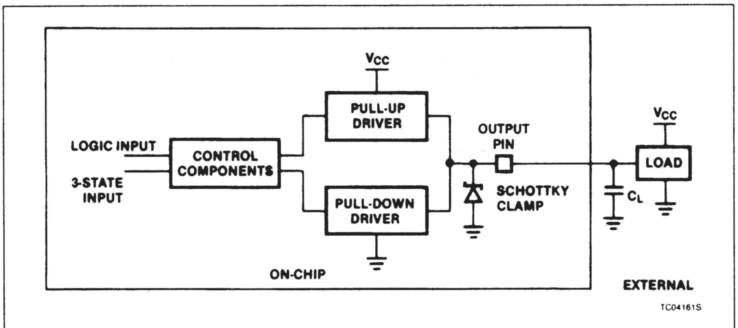


Figure 6. Output Stage Basic Components

ns couples in about 1.0mA of current, enough to switch the input to a Low state for as long as the current lasts. The normal ALS circuit response will be to switch or oscillate. The problem is worse for high-impedance low-capacitance PNP inputs than for Diode inputs. In this case the static voltage to which they float is determined in part by leakage, and is not predictable.

To reiterate, ALS inputs must not be allowed to float. To do so is to invite serious system problems.

OUTPUT CONSIDERATIONS

The purpose of the output stage is to supply current to a load to force it to a High state or to sink current from the load to force it to a Low state. The speed at which the load can be switched from one state to the other depends on how much supply current or sink current is available from the output driver. There must be an amount in excess of that which is required to maintain the static load voltage, and it is the excess current that is available to charge or discharge the load capacitance. Most ALS circuits are designed to fit into one of these categories, based on output drive capability; the normal output stage, the buffer driver which can supply approximately twice as much current, and the high current drivers designed to drive low-impedance terminations.

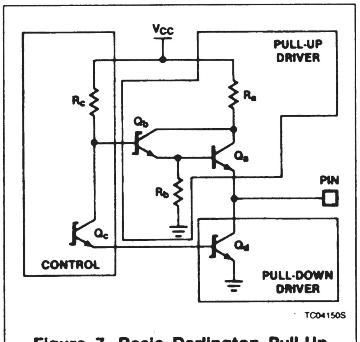


Figure 7. Basic Darlington Pull-Up

Both normal drivers and buffers may be 3-State, which means that, in addition to Low and High states, they can be forced to a high-impedance OFF state as a third possible choice. This allows multiple components to be connected to a bus simultaneously, with only the single-selected device providing actual drive capability.

The basic components of an output stage are shown in Figure 6.

The pull-down driver components sink load currents to force a Low state at the output pin; the pull-up driver components supply current to force a High state. The control components turn on the selected driver and turn off the nonselected driver in response to the logic input signal. For 3-State parts, the control components turn off both drivers if the 3-State control signal is active. The output Schottky clamp is included to suppress inductive undershoots, and is a part of every ALS circuit. The load requires a static current to keep it in either a logic High or Low state. The drivers must also charge and discharge the load capacitance C_L, which is generally one of the major factors that influence switching speed.

Since, to a large extent, they function independently of each other, the pull-up driver, pull-down driver, and control blocks are discussed independently.

PULL-UP DRIVERS

Open-Collector

The simplest pull-up driver consists of no more than a fixed pull-up resistor tied to V_{CC}. For this case, the control stage interacts only with the pull-down driver. In the Low state, this must sink the current from both the pull-up resistor and load. In the High state, the pull-up resistor must supply all of the load current. Most often, the pull-up resistor is not physically part of the integrated circuit chip itself, but is added externally. In this case the only circuit element connected to the output pad (in addition to the ever-present Schottky clamp) is the collector of the pull-down driver transistor, hence the name "Open-Collector." Parts with this output stage can be tied together for bus applications. If any of the connected pull-down stages is active, it will pull the bus Low; only if all of them are off can the external resistor pull the bus High. This action provides a "wired" logical function that is free in the sense that no additional components are required to achieve it.

The Open-Collector output voltage depends on the load, the value of the pull-up resistor, and the voltage to which this is connected. If the resistor value is low, the output will rise to nearly the full value of the pull-up source voltage; in particular, the Open-Collector output can rise to V_{CC}, a voltage higher than that obtainable with a standard Darlington totem-pole pull-up.

Standard Darlington

Most ALS pull-up drivers use dual transistors, connected as shown in Figure 7, with the emitter of the first device Q_b delivering current to the base of the driver Q_a. This configuration is called a Darlington circuit and provides a composite current gain nearly as large as the product of the current gains of Q_b and Q_a.

The major advantage of the Darlington pull-up, as compared to the Open-Collector, is that the pin is actively pulled high by the emitter-follower action of Q_a which is capable of supplying large currents to quickly charge output capacitance. Despite the large output current that is available, the drive requirements of Q_b are low, so that the voltage drop across R_c is small, and the pad will pull up to a voltage nearly as high as $V_{CC} - 2V_{BE}$.

For the case where the output pin voltage is High, the phase-splitter transistor Q_c is off, and the base of Q_b is pulled high by resistor R_c. The current which flows through R_c is just sufficient to provide base drive to Q_b. The base voltage of Q_b will be just slightly below V_{CC}, and the output pin voltage will be less than this by the sum of the V_{BE} drops of Q_b and Q_a, both of which are on. Most of the base current for Q_a and the current through pull-down resistor R_b is supplied from V_{CC} through R_a and Q_b. Q_b has a Schottky clamp to prevent saturation when the current through R_a is large. Resistor R_a limits the amount of current flowing from V_{CC} through Q_a to a value small enough that Q_a will not be damaged if the output pin is accidentally grounded for a short period of time. This short circuit output current is called I_{OS}, and its value is approximately the maximum current

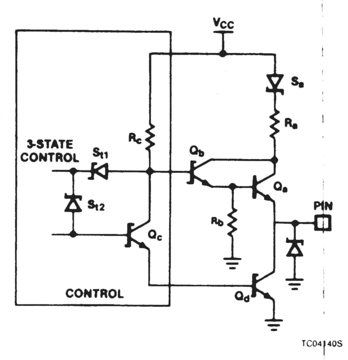


Figure 8. Basic 3-State Pull-Up

available to charge the output capacitance at the beginning of a Low-to-High transition. The minimum current available when the pin has reached the minimum guaranteed high voltage V_{OH} is called output high current (I_{OH}). The maximum output voltage that the pull-up driver can achieve occurs at maximum V_{CC}, and at high temperatures with corresponding low values of transistor V_{BE} and high current gain. Conversely, the minimum high voltage occurs at low V_{CC} and low temperatures.

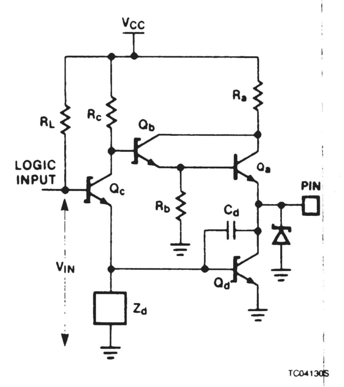


Figure 9. Basic Pull-Down

In the Low state, the pull-down driver Q_d is on and the pin voltage is the Q_d saturation voltage V_{SAT}. Q_c is on and its collector resistor R_c is pulled down to $V_{BE} + V_{SAT}$; the V_{BE} of Q_d, V_{SAT} of Q_c. Q_b is also on, with its emitter at V_{SAT}, and the current through R_b is low. The base-emitter voltage of Q_a is nearly zero and Q_a is off.

Assuming the pull-down is off, the Low-to-High transition speed is governed by: 1) the rate at which R_c can pull-up the base of Q_b; 2) the amount of pin current required to drive the load and charge the load capacitance; 3) the value of R_a; 4) the physical size and current gain of Q_a; and 5) the amount of Q_a base drive current that is lost through R_b to ground.

The pin can be driven above its maximum high value by an external pull-up or by positive reflections from a transmission line. When this happens, Q_a and Q_b do not have sufficient base-emitter drive to keep them on. If the pin voltage rises significantly above V_{CC}, Q_a will begin to leak current into V_{CC}.

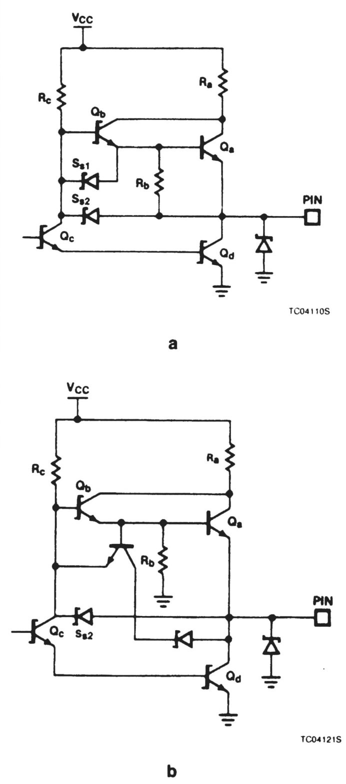
3-State

For all 3-State ALS parts, the leakage paths to a grounded V_{CC} pin are blocked with Schottky diodes. A typical 3-State pull-up is shown in Figure 11. S_a is the series Schottky blocking diode. 3-State Schottkys S_{t1} and S_{t2} serve to simultaneously turn off the pull-up and pull-down drivers. The 3-State control is active when it is pulled low to within V_{SAT} of ground. In this state it sinks all the available drive current for Q_b and Q_c, and pulls their bases down to ($V_{SAT} + V_{Schottky}$), which is essentially one V_{BE}. The voltage drop across R_c is large and 3-State power dissipation is typically high. Q_a and Q_b are off for normal TTL voltage ranges of the output pin; a negative undershoot large enough to drive the pin about one V_{BE} below ground will allow them to turn on and supply current from V_{CC}; this action aids the clamping Schottky diode in preventing the pin voltage from falling lower.

PULL-DOWN DRIVERS

The basic pull-down driver is shown in Figure 9. Q_d is the pull-down driver transistor, a big Schottky-clamped device capable of sinking large currents. C_d is the stray base-collector capacitance of Q_d, and its unavoidable presence has an important effect on the performance of the pull-down driver. Q_c is the Schottky-clamped phase splitter. It functions as a current-limited, low-impedance driver for Q_d when the logic input voltage V_{IN} is high, and as an inverting driver for pull-up Q_b by virtue of the current through R_c when V_{IN} is low and Q_C is off. Z_d is the pull-down impedance network which insures that Q_d is off when V_{IN} is low.

Switching to the logic Low state occurs when V_{IN} is larger than the V_{BE} drops of Q_c plus Q_d, both of which are initially on. Part of the total emitter current available from Q_c comes from R_c, which has a voltage drop of $V_{CC} - V_{BE} - V_{SAT}$. The remainder of the Q_c emitter current is supplied through its base Schottky clamp or by other components not shown in Figure 9 but discussed in the section on control components. A portion of the total Q_C emitter current is lost in the pull-down network Z_d; the remainder is available as base current for pull-down driver Q_d. The amount of current Q_d can sink depends on its base drive, its current gain, and its collector voltage. This current is specified on a per-part basis in the data sheets. Several innovative circuit improvements that increase the drive current for Q_d are shown in Figures 10a and 10b. Speed-up Schottky diodes S_{s1} and S_{s2} have been added to the standard pull-down circuit as shown in Figure 10a. Both are reverse-biased and off in the High state, since R_c pulls the collector of Q_c nearly to V_{CC}. Both connect the collector of Q_c to nodes that need to be discharged during a High-to-Low transition. S_{s1} to the base of Q_a, S_{s2} to



a

b

Figure 10

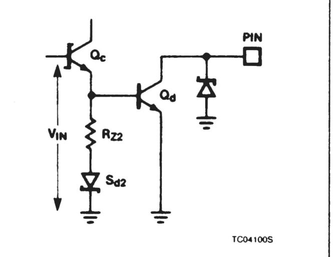


Figure 11

the pin. They will conduct if these node voltages are higher than $V_{BE} + V_{SAT} + V_{Schottky}$, or approximately $2V_{BE}$; they are quite effective above $2V_{BE}$. Figure 10b shows a dynamic kicker that gives an impulse of current which is especially useful in discharging high capacitive loads.

The network of elements labeled Z_d in Figure 9 is the pull-down impedance which insures that Q_d is off when the value of V_{IN} falls below $2V_{BE}$. When the voltage at the base of Q_d is being pulled high by Q_c or low by Z_d, the output pin voltage responds by moving in the opposite direction. This produces a change in voltage across C_d, which is the sum of the base voltage change and the collector voltage change, so the amount of charge required by C_d is magnified by a factor which is larger than unity.

This well-known Miller-effect causes the apparent value of C_d, as perceived by the drivers, to be a factor of about five times larger than the already large physical junction capacitance, all of which means that the drivers Q_c and Z_d need to supply or sink much more current during an output transition than is necessary to maintain static conditions. When static conditions do exist internally in the circuit, noise voltage spikes on the output pin, V_{CC}, or ground can momentarily force the base of Q_d in the direction to produce an output glitch, and the drivers must respond quickly to counter this coupled noise.

A simple Zd element is a resister R_{z2} and a series Schottky diode to ground. This is shown in Figure 11. The Q_d base voltage cannot pull below a Schottky drop, so that switching speed is unimpaired.

CONTROL COMPONENTS

This section covers 3-State control drivers, special 3-State problems, and V_{CC} turn-on current and 3-State glitches during power-up.

3-State Control Drivers

The normal TTL 3-State scheme is shown in Figure 8. The 3-State control voltage in the OFF state is high enough that S_{t1} and S_{t2} are reverse-biased; in the active state the control voltage is low, usually V_{sat}, so that the $Q_a - Q_b$ base emitter stack is off, as is the $Q_c - Q_d$ stack. In the 3-State mode, R_c is dissipating maximum power. Blocking Schottky diode S_a prevents current from flowing backwards through Q_a if the V_{CC} pin is grounded; the output pin high voltage can be about 4.5V before there is any significant 3-State leakage current.

There are several innovative improvements to the basic 3-State circuit, as shown in Figure 12. The addition of inverter $Q_{c2} - R_{c2}$ with a blocking Schottky S_{c2} allows the addition of feedback diodes S_{s1} and S_{s2} to increase I_{AV}; S_{c2} cannot be included in series with R_{c1} because its forward voltage drop would lower V_{OH}. 3-State power is not increased, since only one R_{c1} is pulled low. The current through Q_{c2} is available as added base drive to Q_d, so nothing is wasted. An additional transistor may be paralleled with Q_{c1} and Q_{c2} to control an active pull-down version of impedance Z_d.

I_{CC} Considerations

There is no formal family specification that limits the amount of V_{CC} current an ALS circuit may draw during turn-on as V_{CC} rises from zero to 4.5V. However, an effort has been made to limit maximum turn-on I_{CC} to 110% of I_{CCmax}. This precaution prevents an undesirable system situation where the V_{CC} power supply is large enough to drive the devices, but can't power them up. The major component of turn-on current is V_{CC} to ground feed-through of output stages. Unless specific steps are taken to prevent it, the pull-up Darlington turns on if V_{CC} is greater than $2V_{BE}$, and remains on until the on-chip voltage is high enough to set the phase splitter solidly in one or the other of its two states. The solution is to incorporate extra circuit components that will set the phase splitter at voltages nearly as low as $2V_{BE}$, or turn off the top device with a separate 3-State type structure which activates at low V_{CC} voltages and becomes inoperative when V_{CC} is high.

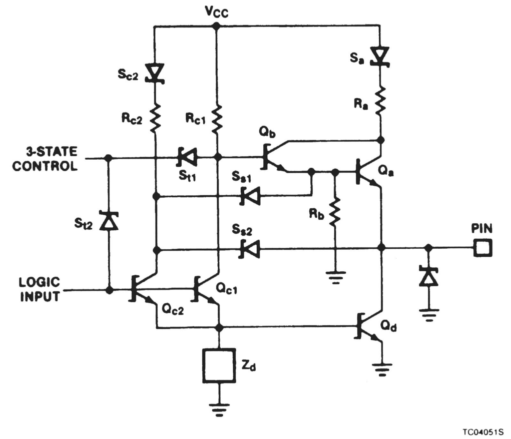


Figure 12. Improved 3-State Circuit

The amount of current that can be fed from an output pin back into a grounded V_{CC} pin, or through the chip to ground for an open V_{CC} pin, depends on the design. Generally, 3-State feedback current is specifically limited to low values which are leakage or breakdown related. Other parts have medium current.

Most 3-State parts, especially selected buffer functions, have additional circuit elements to insure that as they power on they source or sink no appreciable output current, provided that the 3-State control pins are in the active state as V_{CC} rises. This means that V_{CC} can be turned on or off at will in the system to conserve power, and bus voltages will not be affected. Parts with this capability are identified in the specific data sheets.

GROUND VOLTAGE AND OTHER NOISE PROBLEMS

Ground Voltage As A Serious Problem

Excessive ground noise voltage in a system usually produces serious degradation of switching speed. It may also produce unwanted glitches on outputs, or spurious clocks which cause flip-flops to lose data, or relaxation oscillations that completely disrupt a system. It is, without doubt, one of the major causes of logic systems failure ... difficult to accommodate, and difficult to eliminate.

Well planned PC board layout is vital, and multilayer boards with ground and V_{CC} planes are often desirable. Great care must be taken to insure adequate bypassing for V_{CC}. The problems are not trivial, but they can be solved satisfactorily.

Sources Of Ground Noise

Ground lead inductance is the source of most ground noise voltage; it causes a voltage drop proportional to the rate at which the current through it changes.

Inductance is a measure of the amount of energy stored in the magnetic field associated with a current. Low values of inductance imply low energy, which means low voltage required to affect a change in current. As a general rule, inductance decreases as current is allowed to spread out in space, and current interactions decrease. The inductance of a thin wire far removed from the return current path is high; that of a large conductor coaxially encircled by the return path is low. Inductance tends to increase faster than linearly with conductor length, but only approximately logarithmically with decreasing cross-section dimensions. From a logic system viewpoint, ground planes are better than ground traces; wide lines are better than narrow lines; close spacing to planes is good; loops that allow magnetic flux linkages are bad; wire lengths of fractions of inches count; and sockets with long pins add significant inductance to a PC card.

Ground noise voltage is increased by feed-through current spikes. These occur when both top and bottom devices of the output totem-pole driver are on simultaneously, and heavy currents are allowed to flow directly from V_{CC} to ground. They can be minimized in one of two ways: drive the devices such that one is turned off before the other can turn on, or more commonly, drive them together, but very fast, so the feed-through current can flow for only a short time.

Although most ground noise results from ground inductance, resistance also contributes. Static ground offsets unrelated to rates of current change occur, and add to the total ground voltage. Generally speaking, those measures which reduce ground inductance also reduce ground resistance.

Estimating The Magnitude Of Ground Noise

The accurate modeling of ground noise-related problems in logic design is a complex procedure that requires numerical analysis to determine system currents and voltages as a function of time. This can only be accomplished in a satisfactory manner if one has reasonable electrical models, especially for input stages and output drivers of the integrated circuits used in the system. Signetics is prepared to assist customers in solving the sometimes formidable problems associated with large system simulation.

The following discussion derives the minimum peak-value of ground noise that will occur as an integrated circuit discharges a capacitor through ground lead inductance. It points out the minimum problems that will exist. In the real world, the peak ground voltage will always be larger than the simple derivation predicts.

The load capacitor C and its discharge path are shown in Figure 20. The capacitor has been previously charged to a positive voltage, and is discharging through pull-down transistor Q_d and lead ground inductance L_g. As the current changes, it develops a ground voltage V_g across L_g that is equal to the product of L_g times the rate at which it changes.

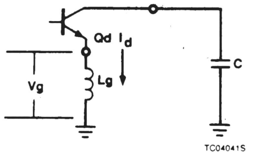


Figure 13

The discharge current I_d will vary with time; starting from zero, it will increase to a maximum value, and then eventually return to zero. There are an infinite number of ways I_d can vary, depending on how the transistor allows charge to flow at any instant in time, but each of the possible current-vs-time discharge curves must define the same area, equal in value to the total charge Q that is removed from the capacitor as its voltage falls by an amount V.

The voltage drop V_g across the inductor at any instant in time will be determined by the slope of the current-vs-time curve, that is, by the rate at which current is changing. The unique curve that has the required area and minimum slope is triangular, as shown in Figure 14. The ground voltage for this case is a square wave as shown in Figure 15. It will be positive while the current is increasing, and negative when the current is decreasing.

The equations of interest in estimating V_g are:

$$\text{Charge} = Q = CV = I_{MAX}\frac{T}{2} = \text{triangle area}$$

$$\text{Ground voltage} = V_g = (\text{triangle slope})(L)$$

$$= \frac{2\ I_{MAX}\ L}{T}$$

Combining the two equations to eliminate I_{MAX} gives:

$$V_g = \frac{4CVL}{T^2}$$

This lower limit of peak ground voltage will always be exceeded in the real world, where ground voltages are usually spikes, not square waves. If a spike is large enough and long enough, the chip will erroneously recognize it as a valid input, and respond either by glitching, slowing down, clocking incorrectly, or oscillating.

An example using values typical for an ALS circuit in a 16-pin DIP illustrates the potential for trouble. If the circuit discharges one standard ALS load of 50pF in 2ns with a voltage change of 3V through a ground inductance of 10nH, the minimum ground voltage will be:

$$V_g = \frac{4 \times 50 \times 10^{-12} \times 3 \times 10 \times 10^{-9}}{(2 \times 10^{-9})^2}$$

$$= 1.5V$$

This value is high, and suggests that if transition times are not to be seriously degraded, inductances must be kept as small as possible, and loads must be minimized.

Effects Of Ground Noise On Input Stages

ALS input voltages are referenced to system ground as illustrated in Figure 16 which shows an equivalent input and output stage. The equivalent input circuit is represented by R_{IN} and the four diodes D1 through D4. These components establish an input switching threshold voltage of 2 V_{BE} relative to chip ground. The on-chip voltage V_{IN} must be different from this value by a margin large enough to guarantee a static Low or High with sufficient overdrive to insure switching speed. The on-chip voltage V_{IN} that is actually available is the difference between the input pin voltage V_{PIN} and the total ground voltage noise V_g. V_g is the sum of the steady state voltage due to ground current flowing through R_g, and the inductive voltage drop across L_g. The inductive voltage is usually the larger of the two, and since it depends on current changes, it will have both positive and negative polarities for each switching cycle. This means that either Low or High input voltages which are too close to switching threshold will allow the noise margin to be exceeded, and if the ground voltage noise persists long enough, the input will switch erroneously. The result of this depends on the chip function. Combinatorial logic usually slows down or produces output glitches. Latches and flip-flops may be clocked inadvertently, and stored data will be lost. Complex circuits that have multiple outputs may oscillate, particularly if one polarity of ground noise results in a rapid change of ground current that produces the opposite polarity ground noise.

Ground noise adds a dimension of difficulty in measuring input threshold voltage. ALS parts are guaranteed to have input thresholds between the limits 0.8V and 2.0V. A typical method of verifying this is to determine the voltage at which the input actually switches. This requires some care, since the true threshold voltage is masked by any noise voltage contributed by the test system or ground inductance. For accurate results, the input pin voltage should approach the switching threshold slowly and smoothly. At threshold the input will switch. Sensing this point is easy for those circuits where an output also switches, glitches, or oscillates. It is much harder to sense this point for those circuits where an input change produces no output change, for example, with flip-flops which change state only when clocked. The input switch point for these devices can be inferred by measuring the input current as a function of input voltage. Clocking the part may produce enough ground noise to distort the measurement, even if the output doesn't switch.

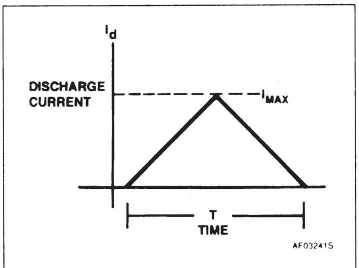


Figure 14

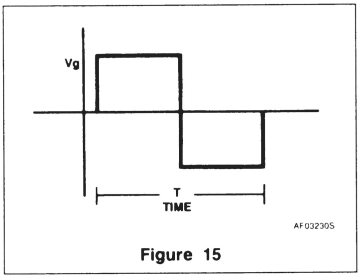


Figure 15

Effects Of Ground Noise On Output Stages

The most obvious effect that ground noise has on output stages is to directly change the voltage available to force discharge current through the pull-down device. If the only source of ground voltage is from the particular output of interest, the ground and output pin inductances will always slow down a High-to-Low transition. They produce a voltage in opposition to the output pin voltage at the beginning of the discharge when currents tend to be high and voltage changes rapidly. As discharge continues, the available drive decreases, and currents increase less rapidly. Eventually the current begins to fall, and the ground voltage reverses polarity, which tends to limit the rate at which the current decreases. If currents have been high, and the inductances are large, there may be substantial undershoot at the end of the switching cycle which can drive the output pin below ground.

If multiple outputs are switching simultaneously, the total ground noise needs to be considered to determine the result for a particular output. For this case, it can happen that ground noise will, in fact, speed up an output; on the other hand, it may introduce delays that are much larger than those possible with single output switching. This behavior makes it difficult to predict, except on a case by case basis, what the actual effects of multiple output switching will be. Curves of delay vs multiple switching have been published, but these serve only as rough guides to indicate potential problems, and need to be backed up with actual analysis for any particular application.

In addition to the direct influence on discharge voltage, excessive ground noise can affect the operation of the control components, and alter both rise and fall times by driving pull-up or pull-down stages incorrectly. One example of this can be understood with reference to Figure 17. The scenario is that the output pin is Low, but on the verge of switching High, with V_{IN} falling and Q_c ready to turn off. A problem occurs if, at the instant before the pull-up transistor Q_a turns on to pull the output pin high, the voltage from output pin to chip ground falls. This can happen as a result of inductive undershoot driving the output pin down, or by a rise in ground voltage caused by currents completely unrelated to the output of interest. The low output-pin-to-chip-ground voltage pulls down the emitter of Q_c through Schottky clamp diode S_d, and if V_{IN} is not low enough to counteract this, Q_c will not turn off. The net result is that R_c cannot rise, and the transition is delayed until the noise voltage from output to ground disappears.

V_{CC} Noise As An Additional Problem

Inductance in the V_{CC} lead produces noise in the on-chip V_{CC} voltage that is entirely analogous to ground voltage. The effects of V_{CC} noise can be nearly as harmful as those produced by ground noise, the only significant difference being the fact that TTL input voltages are referenced to ground instead of V_{CC}.

The first symptom of excessive V_{CC} inductive voltage drop is a change in the edge rate for a Low-to-High transition. This will decrease if the on-chip V_{CC} falls, and increase if it rises. If the ground to V_{CC} voltage falls below a minimum value, internal circuit delays or glitches can occur, and functions with flip-flops or other storage elements may lose data. As is the case with excessive ground noise, ALS circuits may break into relaxation oscillation.

Because V_{CC} to ground voltage must remain above a minimum value to avoid logic errors and glitches, it is absolutely vital that V_{CC} to ground bypassing is adequate. This requires low inductance V_{CC} and ground PC traces, and low inductance bypass capacitors. ALS parts are guaranteed to function properly for low V_{CC} of 4.5V. This means that pin voltages must not fall below this value for any appreciable time: fractions of nanoseconds. V_{CC} system voltage should be close to the maximum guaranteed value for safe system design.

Designing To Reduce The Effects Of Ground Noise

The typical 1.5V minimum value for ground noise, calculated in the preceeding example, points out the possibility of noise-related problems when only one standard 50pF load is being driven by an output stage. Simultaneous switching of more than one such load obviously increases the risk of trouble, and raises the question of how an octal part can

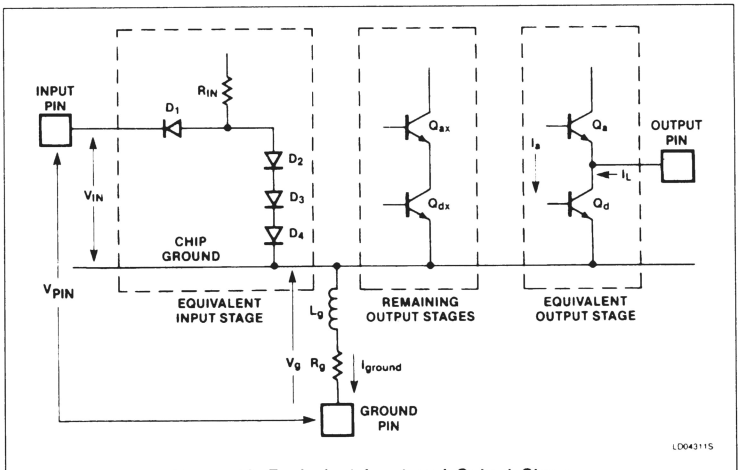


Figure 16. Equivalent Input and Output Stage

work at all. Fortunately, the real world, with careful PC layout, is not usually so grim.

The standard 50pF load is a lot of capacitance, chosen so one can estimate the chip response for a single output switching under conditions that approach worst case. On a modern PC board a wire trace that has 50pF stray capacitance is several feet long and looks like a resistive delay line instead of a lumped capacitor.

Traces on a PC card must be short to behave like lumped capacitance for an output stage. For this case, a major contributor to driver current is the load presented by the input stages of the driven circuits, and the associated stray capacitance. As previously mentioned, the input current for ALS parts is related to edge rates, and is generally larger than the measured static value of input capacitance would predict. Because of this, the useful fan-out of ALS circuits may be more dependent on ground noise of drivers with heavy capacitive loads than on the amount of current available to a static DC load, which is the guaranteed data sheet value.

Most of Signetics' ALS parts are available in surface mount packages, and these have lower ground inductance than the standard DIP parts.

Inductance of output signal pins reduces the rate at which associated ground current can change, and this reduces ground noise voltage without a corresponding reduction of static output voltage. This inductance may be intentionally increased by adding trace length on the PC board; one needs to be careful, and anticipate the increase in output ringing during switching transitions.

In summary, there are many potential problems that one can anticipate in logic systems with fast edge rates. Some of these are dependent on the available components and their respective packages, and the system designer must be certain that the demands made of them are not more than they can handle. A second major consideration is the system layout, especially from the standpoint of ground, V_{CC}, and signal lead inductance.

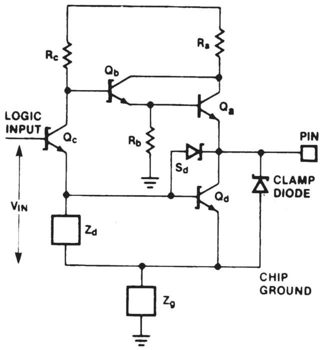


Figure 17

Section 4
ALS Users' Guide

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Design Considerations 4–11

Data Sheet Specification Guide

INTRODUCTION

Signetics' ALS data sheets have been configured for quick usability.

They are self-contained and should require minimum reference to other sections for amplifying information.

TYPICAL PROPAGATION DELAY AND SUPPLY CURRENT

The typical propagation delays listed at the top of the data sheets are the average between t_{PLH} and t_{PHL} for the most significant data path through the part.

In the case of clocked products, this is sometimes the maximum frequency of operation. In any event, this number is under the operating conditions of $V_{CC} = 5.0V$ and $T_A = 25°C$.

The typical I_{CC} current shown in that same specification block is the average current (in the case of gates, this will be the average of the I_{CCH} and I_{CCL} currents) at $V_{CC} = 5.0V$ and $T_A = 25°C$. It represents the total current through the package, not the current through the individual functions.

LOGIC SYMBOLS

There are two types of logic symbols. The conventional one, "Logic Symbol," explicitly shows the internal logic (except for complex logic). The other is "Logic Symbol (IEEE/IEC)" as developed by the IEC and IEEE. The International Electrotechnical Commission (IEC) has developed a very powerful symbolic language than can show the relationship of each input of a digital logic circuit to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 817-12) that will consolidate the original work started in the mid-1960's and published in 1972 (Publication 117-15), and the amendments and supplements that have followed. Similarly, for the U.S.A., IEEE Committee SCC 11 has revised the publication IEEE Std 91/ANSI Y32.14-1973.

The updated version IEEE Standard Graphic Symbols for Logic Functions ANSI/IEEE Std 91-1984 (Revision of ANSI/IEEE Std 91-1973 [ANSI Y32.14-1973]) can be ordered through:

IEEE Service Center
445 Hoes Lane
Piscataway, New Jersey 08854
Phone (201) 981-0060

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it. There is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than −0.5V is applied to the output pin, after that voltage is removed, the part will still be functional and its useful life will not have been shortened.

Input and output voltage specifications in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (−0.5V).

Absolute maximum ratings imply that any transient voltages, currents, and temperatures will not exceed the maximum ratings. Absolute maximum ratings are shown in Table 1.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has a dual purpose. It sets environmental conditions (operating free-air temperature), and it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteristics tables.

Some care must be used in interpreting the numbers in these tables. Signetics feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment ... if V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by DC Electrical Characteristics table. There is a tendency

Table 1. ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		74F	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	Standard outputs	16	mA
		3-State and buffer outputs	48	mA
		−1 version outputs	96	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature range		−65 to +150	°C

on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionality in a "truth-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the part has assumed its final and correct output state. Thus, V_{IH} and V_{IL} should never be used in testing the functionality of any ALS part type. For these types of tests, input voltages of +4.5V and 0.0V should be used for the High and Low states, respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" Highs and Lows during functional testing is done primarily to reduce the effects of the noise typically present at the test heads of automated test equipment especially when using cables that may at times reach several feet. The situation in a system on a PC board is less severe than in a noisy production environment. Typical recommended operating conditions are shown in Table 2.

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Signetics during their testing operations conducted under the conditions set forth in the Recommended Operating Conditions table.

V_{OH} and V_{OL} values vary depending on the V_{CC} values specified and the type of output structure; standard, 3-State, or buffer. Generally, as the output current and V_{CC} variations increase, the guaranteed minimum V_{OH} decreases and the maximum V_{OL} increases. Signetics specifies and tests V_{OH} and V_{OL} for 10% V_{CC} swings.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at a guaranteed minimum input breakdown voltage. The test conditions for I_I vary according to the type of input structure being tested. PNP and Diode inputs are tested with V_{CC} = MAX and 7.0V at the input. When I_I is being measured on transceiver I/O pins, both V_{CC} and the input voltage are 5.5V. The reduced input voltage is necessary because of the output structure connected to the input structure. Output structures break down sooner than input structures and it is impossible to test the input without testing the output also.

I_{IH} for both Diode and PNP input structures is less than 20μA typically. I_{IL} is less than 100μA for PNP inputs and less than 200μA for Diode inputs. If multiple input structures are tied together in the design, then the input current values also multiply.

For transceiver I/O pins the outputs are in the High-impedance state when the inputs are tested. Therefore, the small amount of extra leakage is combined with the I_{IH} and I_{IL} specifications.

I_{OZH} is tested with setup conditions that would put the output in the High state if it were not in the 3-State High-impedance condition. I_{OZL} is similar except the setup condition is for the Low state.

I_{OH} is tested only on Open-Collector outputs as a leakage test for the lower output transistor structure. V_{CC} is less than V_{OH} so that there is not a current path to or from V_{CC} that would mask the leakage.

IO is approximately one half of the true short-circuit output current value. It is measured at ½ V_{CC} in a linear region of the low-state output current characteristics. This method of testing allows indirect measurement of the current available for capacitive load charging while avoiding test problems of over-heating and potential circuit damage associated with IOS tests.

DC electrical characteristics are shown in Table 3.

AC ELECTRICAL CHARACTERISTICS

The AC Electrical Characteristics table (see Table 4) contains the guaranteed limits when tested under the conditions set forth in the AC Test Circuits and Waveforms section. In some cases, the test conditions are further defined by the AC setup requirements (see Table 5) — this is generally the case with counters and flip-flops where setup and hold times are involved.

All of the AC characteristics are guaranteed with 50pF load capacitance. The reason for choosing 50pF over 15pF as load capacitance is that it allows more leeway in dealing with stray capacitance, and also loads the device during rising or falling output transitions, which more closely resembles the loading to be expected in average applications, thus giving the designer more useful delay figures.

Table 2. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage	Open-Collector			5.5	V
I_{OH}	High-level output current	Standard			−0.4	mA
		3-State			−2.6	mA
		Buffers			−15	mA
I_{OL}	Low-level output current	Standard			8	mA
		3-State and Buffers			24	mA
		−1 versions			48	mA
T_A	Operating free-air temperature range		0		70	°C

Although the 50pF load capacitance will increase the propagation delay by an average of about 1ns for ALS devices, it will increase several ns for standard Schottky devices.

The load resistor of 500Ω is conveniently specified as both a pull-up and pull-down load resistor.

ALS products are being released in the surface-mounted SO package as a commercial option.

Table 3. DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER[1]		CONDITIONS[2]	LIMITS[2]			UNITS	V_{CC}[4]
				Min	Typ[3]	Max		
V_{IK}	Input clamp diode voltage		$I_{IN} = -18mA$			-1.5	V	MIN
V_{OH}	Output High voltage	Std.[5]	$I_{OH} = -0.4mA$	$V_{CC}-2$			V	5V ± 10%
		3-State	$I_{OH} = -2.6mA$	2.4	3.2		V	MIN
			$I_{OH} = -3mA$	2.4	3.2		V	MIN
		Buffers	$I_{OH} = -15mA$	2.0			V	MIN
V_{OL}	Output Low voltage	Std.[5]	$I_{OL} = 4mA$		0.25	0.4	V	MIN
			$I_{OL} = 8mA$		0.35	0.5	V	MIN
		3-State and Buffers	$I_{OL} = 12mA$		0.25	0.4	V	MIN
			$I_{OL} = 24mA$		0.35	0.5	V	MIN
		-1 version	$I_{OL} = 48mA$		0.35	0.5	V	4.75V
I_I	Input High current breakdown test	Diode inputs	$V_{IN} = 7.0V$			100	μA	MAX
		PNP inputs	$V_{IN} = 7.0V$			100	μA	MAX
		Transceiver I/O pins	$V_{IN} = 5.5V$			100	μA	5.5V
I_{IH}	Input High current		$V_{IH} = 2.7V$ (20μA × n High U.L.)			n(20)	μA	MAX
I_{IL}	Input Low current	Diode inputs	$V_{IL} = 0.4V$ (-0.2mA × n Low U.L.)			n(-0.2)	mA	MAX
		PNP inputs	$V_{IL} = 0.4V$ (-100μA × n Low U.L.)			n(-100)	μA	MAX
I_{OZH}	3-State OFF current High		$V_{OUT} = 2.7V$			20	μA	MAX
I_{OZL}	3-State OFF current Low		$V_{OUT} = 0.4V$			-20	μA	MAX
I_{OH}	Open-Collector output leakage		$V_{OH} = 5.5V$			100	μA	MIN
I_O[6]	Output current		$V_{OUT} = 2.25V$	-30		-112	mA	MAX

NOTES:

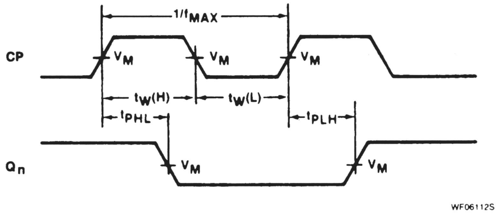
1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to $T_A = +25°C$ and $V_{CC} = +5.0V$.
4. MIN and MAX refer to the values listed in the data sheet table of recommended operating conditions.
5. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-State outputs.
6. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit current, I_{OS}.

Table 4. AC ELECTRICAL CHARACTERISTICS

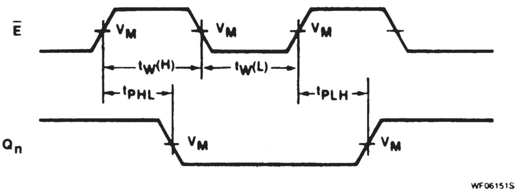
SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		UNIT
				Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74ALS373	Waveform 2	2.0 2.0	12.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 1	3.0 3.0	14.0 14.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.0 3.0	14.0 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	10.0 12.0	ns
f_{MAX}	Maximum clock frequency	74ALS374	Waveform 1	50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	3.0 4.0	12.0 14.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 4 Waveform 5	3.0 3.0	14.0 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	2.0 3.0	10.0 12.0	ns

Table 5. AC SETUP REQUIREMENTS

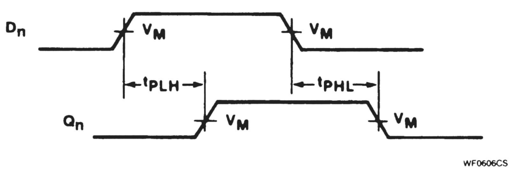
SYMBOL	PARAMETER		TEST CONDITION	LIMITS $T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		UNIT
				Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_n to E	74ALS373	Waveform 3	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E		Waveform 3	6.0 6.0		ns
$t_w(H)$	E Pulse width, High		Waveform 1	10.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_n to CP	74ALSF374	Waveform 3	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		Waveform 3	1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	10.0 10.0		ns


1/fMAX
CP
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Qn
VM
VM
WF06112S

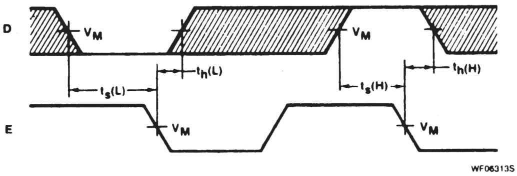
Waveform 1. Clock to Output Delays and Pulse Width


E
VM
VM
VM
tW(H)
tW(L)
tPHL
tPLH
Qn
VM
VM
WF06151S

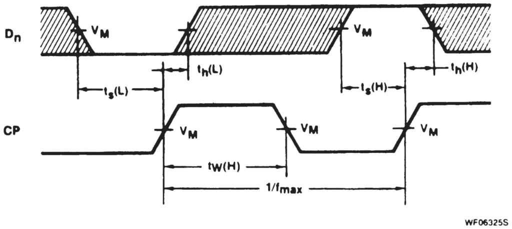
Waveform 2. Latch Enable to Output Delays and Latch Enable Pulse Width


Dn
VM
VM
tPLH
tPHL
Qn
VM
VM
WF0606CS

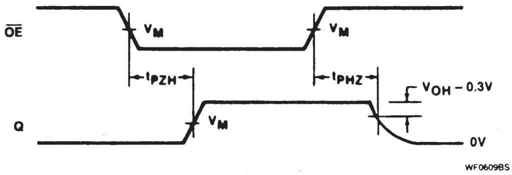
Waveform 3. Propagation Delay Data to Q Outputs


D
VM
VM
th(L)
th(H)
ts(L)
ts(H)
E
VM
VM
WF06313S

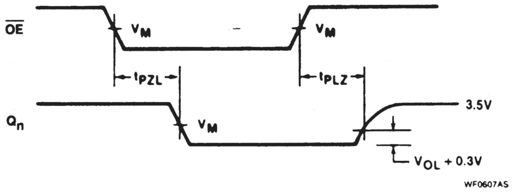
Waveform 4. Data Setup and Hold Times


Dn
VM
VM
th(L)
th(H)
ts(L)
ts(H)
CP
VM
VM
VM
tW(H)
1/fmax
WF06325S

Waveform 5. Data Setup and Hold Times


OE
VM
VM
tPZH
tPHZ
VOH – 0.3V
Q
VM
0V
WF06098S

Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level


OE
VM
VM
tPZL
tPLZ
Qn
VM
3.5V
VOL + 0.3V
WF0607AS

Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, $V_M = 1.3V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. AC Waveforms

TEST CIRCUITS AND WAVEFORMS

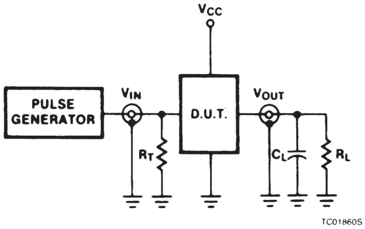
The 500Ω load resistor, R_L to ground, as described in Figure 2, acts as a ballast to slightly load the totem-pole pull-up and limit the quiescent High state voltage to about +3.5V. Otherwise, an output would rise quickly to about +3.5V, but then continue to rise very slowly up to about +4.4V. On the subsequent High-to-Low transition, the observed t_{PHL} would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the Low state. Perhaps, more importantly, the 500Ω resistor to ground can be a high-frequency, passive probe for a sampling scope, which costs much less than the equivalent high-impedance probe. Alternatively, the 500Ω load to ground can simply be a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω termination of the scope completing the path to ground. Note that with this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

Figure 3, Test Circuit for 3-State Outputs, shows a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with Open-Collector outputs and for measuring one set of the Enable/Disable parameters (Low-to-OFF and OFF-to-Low) of a 3-State output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establish a quiescent High level of +3.5V, which correlates with the High level discussed in the preceding paragraph.

As shown in Figure 1, AC Waveforms, the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from the quiescent level (i.e., Low for t_{PLZ} or High for t_{PHZ}).

Since the rising or falling waveform is RC-controlled, the 0.3V of change is more linear and is less susceptible to external influences.

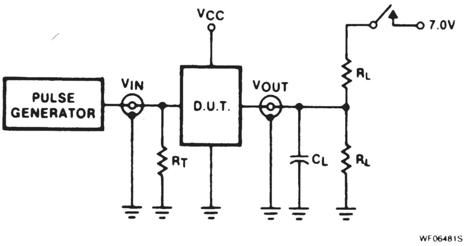
More importantly, from the system designer's point of view, 0.3V is adequate to ensure that a device output has turned OFF. It also gives system designers more realistic delay times to use in calculating minimum cycle times.



DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 2. Test Circuit for Totem-Pole Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PLZ}	closed
OC	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 3. Test Circuit for 3-State and Open-Collector (OC) Outputs

Good, high-frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.0ns, and signal swing of 0V to +3.5V, 1.0MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

Data Sheet Specification Guide

DC SYMBOLS AND DEFINITIONS

Voltages — All voltages are referenced to ground. Negative-voltage limits are specified as absolute values (i.e., −10V is greater than −1.0V).

V_{CC}	**Supply voltage:** The range of power supply voltage over which the device is guaranteed to operate within the specified limits.
V_{IKMax}	**Input clamp diode voltage:** The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.
V_{IH}	**Input High voltage:** The range of input voltages recognized by the device as a logic High.
V_{IHMin}	**Minimum input High voltage:** This value is the guaranteed input High threshold for the device. The minimum allowed input High in a logic system.
V_{IL}	**Input Low voltage:** The range of input voltages recognized by the device as a logic Low.
V_{ILMax}	**Maximum input Low voltage:** This value is the guaranteed input Low threshold for the device. The maximum allowed input Low in a logic system.
V_M	**Measurement voltage:** The reference voltage level on AC waveforms for determining AC performance. Usually specified as 1.3V for the ALS family.
V_{OHMin}	**Output High voltage:** The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.
V_{OLMax}	**Output Low voltage:** The maximum guaranteed Low voltage at an output terminal sinking the specified load current I_{OL}.
V_{T+}	**Positive-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T-} (Min).
V_{T-}	**Negative-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition falls from above V_{T+} (Max).

Currents — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC}	**Supply current:** The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst-case operation unless specified.
I_I	**Input leakage current:** The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guarantees the minimum breakdown voltage for the input.
I_{IH}	**Input High current:** The current flowing into an input when a specified High-level voltage is applied to that input.
I_{IL}	**Input Low current:** The current flowing out of an input when a specified Low-level voltage is applied to that input.
I_O	**Output current:** The output current that is approximately one half of the true short-circuit output current (I_{OS}).
I_{OH}	**Output High current:** The leakage current flowing into a turned off Open-Collector output with a specified High output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the High state.
I_{OL}	**Output Low current:** The current flowing into an output which is the Low state.
I_{OS}	**Output short-circuit current:** The current flowing out of an output which is in the High state when that output is short circuit to ground.
I_{OZH}	**Output off current High:** The current flowing into a disabled 3-State output with a specified High output voltage applied.
I_{OZL}	**Output off current Low:** The current flowing out of a disabled 3-State output with a specified Low output voltage applied.

AC SYMBOLS AND DEFINITIONS

f_{MAX}	**Maximum clock frequency:** The maximum input frequency at a Clock input for predictable performance. Above this frequency the device may cease to function.
t_{PLH}	**Propagation delay time:** The time between the specified reference points on the input and output waveforms with the output changing from the defined Low level to the defined High level.
t_{PHL}	**Propagation delay time:** The time between the specified reference points on the input and output waveforms with the output changing from the defined High level to the defined Low level.
t_{PHZ}	**Output disable time from High level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the High level to a high-impedance "OFF" state.
t_{PLZ}	**Output disable time from Low level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the Low level to a high-impedance "OFF" state.
t_{PZH}	**Output enable time to a High level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high-impedance "OFF" state to High level.
t_{PZL}	**Output enable time to a Low level of a 3-State output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high-impedance "OFF" state to Low level.

t_h	**Hold time:** The interval immediately following the active transition of the timing pulse (usually the Clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.
t_s	**Setup time:** The interval immediately preceding the active transition of the timing pulse (usually the Clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
t_W	**Pulse width:** The time between the specified reference points on the leading and trailing edges of a pulse.
t_{REC}	**Recovery time:** The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (Clock) pulse input such that the device will respond to the synchronous input.
t_{TLH}	**Transition time, Low-to-High:** The time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from Low to High.
t_{THL}	**Transition time, High-to-Low:** The time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from High to Low.
t_r, t_f	**Clock input rise and fall times:** 10% to 90% value.

Design Considerations

INTRODUCTION

The properties of ALS logic circuits dictate that care be taken in the design and layout of a system.

Some general design considerations are included in this section. This is not intended to be a thorough guideline for designing ALS systems, but a reference for some of the constraints and techniques to be considered when designing a high-speed system.

HANDLING PRECAUTIONS

As described in the Circuit Characteristics section, ALS devices are susceptible to damage from electrostatic discharge (ESD).

- Signetics ALS devices are shipped in conducting foam or anti-static tubes and foil-lined boxes to minimize ESD during shipment and unloading.
- Before opening the shipment of ALS devices, make sure that the individual is grounded and all handling means (such as tools, fixtures, and benches) are grounded.
- After removal from the shipping material, the leads of the ALS devices should always be grounded. In other words, ALS devices should be placed leads-down on a grounded surface, since ungrounded leads will attract static charge.
- Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn on-off, do not exceed absolute maximum ratings.
- After assembly on PC boards, ensure that ESD is minimized during handling, storage or maintenance.
- ALS inputs should never be left floating on a PC board. This precaution applies to any TTL family. As a temporary measure, a resistor with a resistance greater than 10kΩ should be soldered on the open input. The resistor will limit accidental damage if the PC board is removed and brought into contact with static-generating materials.

INPUT CLAMPING

ALS circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes should not be used to clamp negative DC voltages or long-duration, negative pulses.

UNUSED INPUTS

Proper digital design rules dictate that all unused inputs on TTL devices be tied either High or Low. This is especially important with ALS logic.

Electrically-open inputs can degrade AC noise immunity as well as the switching speed of the device. Tying inputs to V_{CC} or GND, directly or through a resistor, protects the device from in-circuit electrostatic damage.

ALS devices do not require an input resistor to tie the input High. Inputs can be connected directly to V_{CC} as well as ground.

Possible ways of handling unused inputs are:

1. Unused active-High NAND or AND inputs to V_{CC}. The inputs should be maintained at a voltage greater than 2.7V, but should not exceed the absolute maximum rating.
2. Connect unused active-High NOR or OR inputs to ground.
3. Tie unused active-High NAND or AND inputs to a used input of the same gate, provided that the High-level fanout of the driving circuit is not impaired.
4. Connect the unused active-High NAND or AND inputs to the output of an unused gate that is forced High.

MIXING ALS WITH OTHER TTL FAMILIES

Mixing the slower TTL families such as 74 and 74LS with the higher speed families such as 74ALS is possible but must be done with caution. Each family of TTL devices has unique input and output characteristics optimized to achieve the desired speed or power features.

The speed/power characteristics of the ALS devices are achieved partially by the internal rise and fall times, as well as those at input and output nodes. These transitions can cause noise of various types in a system. Power and ground line noise are generated by the transitions of the current in the output load capacitance. Signal line noise can also be generated by the output transitions.

The noise generated by ALS devices can be minimized in systems designed with shorter signal lines, good ground planes, well-bypassed power distribution networks, layouts that minimize adjacent signal lines that run parallel, and improved impedance matching in signal lines to reduce transmission line-type reflections.

INPUT LOADING AND OUTPUT DRIVE COMPARISON

The logic levels of all TTL products are fully compatible with each other. However, the input loading and output drive characteristics of each family are different and must be taken into consideration when mixing them in a system. Table 1 shows the relative drive capabilities of each family for commercial temperature and voltage ranges.

INPUT-OUTPUT LOADING AND FAN-OUT TABLE

For convenience in system design, the input-output loading and fan-out characteristics of each circuit are specified in terms of unit loads and actual load value. One ALS Unit Load (U.L.) in the High state is defined as 20μA; thus both the input High leakage current, I_{IH}, and output High current-sourcing capability, I_{OH}, are normalized to 20μA.

Similarly, one ALS Unit Load (U.L.) in the Low state is defined as 0.1mA and both the input Low current, I_{IL}, and the output Low current-sinking capability, I_{OL}, are normalized to 0.1mA.

For added convenience, the actual load value in amperes is listed in the column adjacent to U.L.

CLOCK PULSE REQUIREMENTS

All ALS Clock inputs are buffered to increase their tolerance of slow positive-clock edges and heavy ground noise. Nevertheless, the rise time on positive-edge-triggered devices should be less than the nominal clock-to-output delay time measured between 0.8V to 2.0V levels of the clock driver for added safety margin against heavy ground noise. Not only a fast rising, clean Clock pulse is required, but the path between the clock drive and clock input of the device should be well-shielded from electromagnetic noise.

ALS OUTPUTS TIED TOGETHER

The only ALS outputs that are designed to be tied together are Open-Collector and 3-State outputs. Standard ALS outputs should not be tied together unless their logic levels will always be the same; either all High or all Low. When connecting Open-Collector or 3-State outputs together, some general guidelines must be observed.

Table 1. Loading Comparisons

DRIVEN DEVICE FAMILY		74F	74F (NPN)	74LS	74	74S	74ALS
Driving Device Family	**I_{OL} (Min)**	**I_{IL} (Max)**					
		0.6mA	**20μA**	**0.4mA**	**1.6mA**	**2.0mA**	**0.1mA**
		Maximum Number of Loads Driven					
74F	20mA	33	1,000	50	12.5	10	200
74F (NPN)	64mA	106	3,200	160	40	32	640
74LS	8mA	13	400	20	5	4	80
74LS Buffer	24mA	40	1,200	60	15	12	240
74	16mA	26	800	40	10	8	160
74 Buffer	40mA	78	2,400	120	30	24	400
74S	20mA	33	1,000	50	12.5	10	200
74S Buffer	60mA	100	3,000	150	37.5	30	600
74ALS	8mA	13	400	20	5	4	80
74ALS Buffer	24mA	40	1,200	60	15	12	240
74ALS −1 version	48mA	80	2,400	120	30	24	480

Open-Collector Outputs

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices must have a pull-up resistor (or resistors) added between the OR-tie connector and V_{CC} to establish an active-High level. Only special high-voltage buffers can be tied to a higher voltage than V_{CC}. The minimum and maximum size of the pull-up resistor is determined as follows:

$$R\ (\text{Min}) = \frac{V_{CC}\ (\text{Max}) - V_{OL}}{I_{OL} - N_2\ (I_{IL})}$$

$$R\ (\text{Max}) = \frac{V_{CC}\ (\text{Min}) - V_{OH}}{N_1\ (I_{OH}) + N_2\ (I_{IH})}$$

where: I_{OL} = Minimum I_{OL} guarantee or OR-tied elements.

$N_2\ (I_{IL})$ = Cumulative maximum input Low current for all inputs tied to OR-tie connection.

$N_1\ (I_{OH})$ = Cumulative maximum output High leakage current for all outputs tied to OR-tie connection.

$N_2\ (I_{IH}\ )$ = Cumulative maximum input High leakage current for all inputs tied to OR-tie connection.

If a resistor divider network is used to provide the High level, the R (Max) must be decreased enough to provide the required [(V_{OH}/R (pull-down)] current.

3-State Outputs

3-State outputs are designed to be tied together, but are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-State output should be active at any time. This generally requires that the output enable signals be non-overlapping. When TTL decoders are used to enable 3-State outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally guarantee when the address is changing.

Since most 3-State output enable signals are active-Low, shift registers or edge-triggered storage registers provide good output enable buffers. Shift registers with one circulating Low bit, such as the 'ALS164 is ideal for sequential enable signals. The 'ALS174 or 'ALS273 can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from Low-to-High faster than from High-to-Low, the selection of one device at a time is assured.

GND

Good system design starts with a well thought out ground layout. Try to use ground plane if possible. This will save headaches later on. If ground strip is used, try to reduce ground path in order to minimize ground inductance. This prevents crosstalk problems. Quite often, jumper wire is used for connecting to ground at the breadboarding stage, but a solid ground must be used even at the breadboarding stage.

V_{CC}

Typical dynamic impedance of un-bypassed V_{CC} runs from 50Ω to 100Ω, depending on V_{CC} and GND configuration. This is why a sudden current demand, due to an IC output switching, can cause momentary reduction in V_{CC} unless a bypass (decoupling) capacitor is located near V_{CC}.

Not only is there a sudden current demand due to output switching transient, there is also a heavy current demand by the buffer driver. Assuming the buffer output sees a 50Ω dynamic load and the buffer Low-to-High transition is 2.5V, the current demand is 50mA per buffer. If it is an octal buffer, the current demand could be 0.4mA per package in 3ns time!

The next step is to figure out the capacitance requirement for each bypass capacitor. Using the previously-mentioned octal buffer and assuming the V_{CC} droop is 0.1V, then C is:

$$C = \frac{0.4\text{A} \times 3 \times 10^{-9}\ \text{sec}}{0.1\text{V}} = 12 \times 10\text{F}^{-9}$$

$$= 0.012\mu\text{F}$$

This formula is derived as follows:

$cQ = CV$

by differentiation:

$$\frac{\Delta Q}{\Delta t} = C\frac{\Delta V}{\Delta t}$$

Since $\dfrac{\Delta Q}{\Delta t} = I$

the equation becomes $I = C\ \dfrac{\Delta t}{\Delta t}$

hence, $C = \frac{I\Delta t}{\Delta V}$

Select the C bypass $\geqslant 0.02\mu F$ and try to use a high-quality RF capacitor. Place one bypass capacitor for each buffer and one bypass capacitor every two other types of IC packages. Make sure that the leads are cut as short as possible.

In addition, place bypass capacitors on a board to take care of board-level current transients.

CROSS TALK

The best way to handle cross talk is to prevent it from occurring in the first place; quick-fixes are troublesome and costly. To prevent cross-talk, maximize spacing between signal lines and minimize spacing between signal lines and ground lines. Preferably, place ground lines between signal lines. For added precaution, add a ground trace alongside either the potential cross-talker or the cross-listener.

For backplane or wire-wrap, use twisted pair for sensitive functions such as clocks, asynchronous set or reset, or asynchronous parallel load. In flat cable, make every other conductor ground.

For multilayer P.C. boards, run signal lines in adjacent planes perpendicular to prevent magnetic coupling, and limit capacitive coupling. Use power shield (V_{CC} or ground plane) in between signal planes.

Since any voltage change, noise or otherwise, arriving at the unterminated end of transmission lines double in amplitude, even a partially terminated line reduces the amplitude of the signal (noise or otherwise) appearing at the end of the line; therefore, using a terminating resistor whose value is equal to the line characteristics impedance will help reduce cross-talk.

Section 5

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74ALS00A

Quad 2-Input NAND Gates

Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
H	H	L
L	X	H
X	L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS00A	4.0 ns	1.0 mA

ORDERING INFORMATION

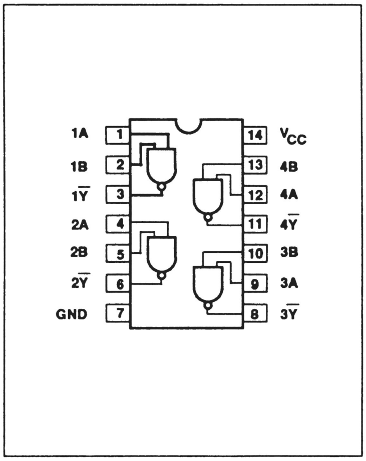
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74ALS00AN
14-Pin Plastic SO	74ALS00AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

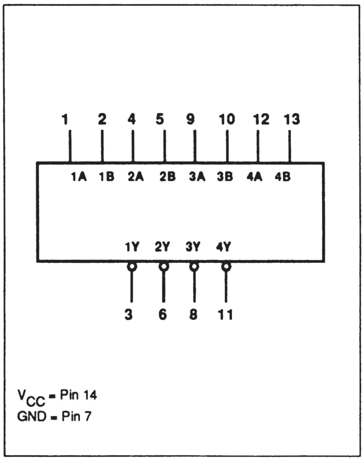
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB	Data inputs	1.0/1.0	20µA/0.1mA
n$\overline{Y}$	Data Output	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

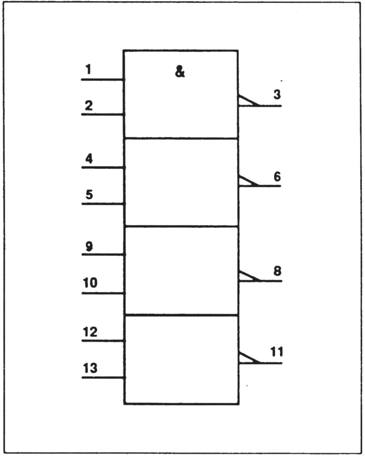
PIN CONFIGURATION


1A 1
1B 2
1$\overline{Y}$ 3
2A 4
2B 5
2$\overline{Y}$ 6
GND 7
14 V_{CC}
13 4B
12 4A
11 4$\overline{Y}$
10 3B
9 3A
8 3$\overline{Y}$

LOGIC SYMBOL


1 2 4 5 9 10 12 13
1A 1B 2A 2B 3A 3B 4A 4B
1Y 2Y 3Y 4Y
3 6 8 11
V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)


&
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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ± 10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC} - 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = 4mA		0.25	0.4	V
			V_{IH} = MIN	I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 0V		0.5	0.85	mA
		I_{CCL}		V_I = 4.5V		1.5	3.0	mA

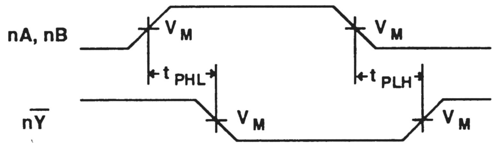
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA or nB to n$\overline{Y}$	Waveform 1	2.0 2.0	11.0 8.0	ns

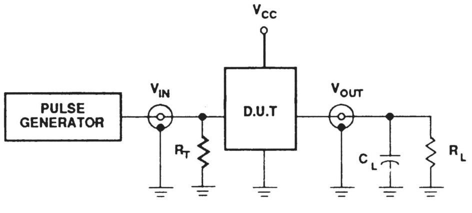
AC WAVEFORM


nA, nB
V_M
t_{PHL}
t_{PLH}
n$\overline{Y}$

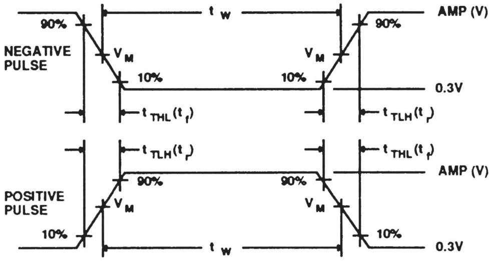
Waveform 1. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
V_{IN}
V_{OUT}
PULSE GENERATOR
D.U.T
R_T
C_L
R_L

Test Circuit for Totem-Pole Outputs


t_w
AMP (V)
90%
NEGATIVE PULSE
V_M
10%
0.3V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
POSITIVE PULSE

V_M = 1.3V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS02

Quad 2-Input NOR Gates

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS02	4.0 ns	1.0 mA

FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	**$\overline{Y}$**
H	X	L
X	H	L
L	L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

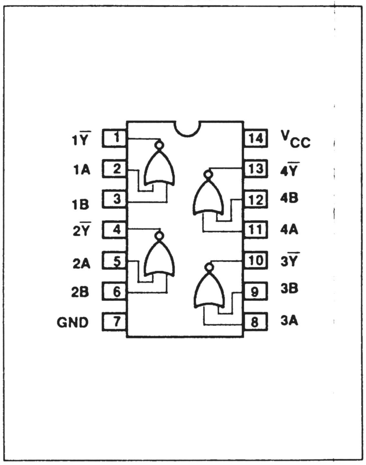
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74ALS02N
14-Pin Plastic SO	74ALS02D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB	Data inputs	1.0/1.0	20μA/0.1mA
n$\overline{Y}$	Data Output	20/80	0.4mA/8mA

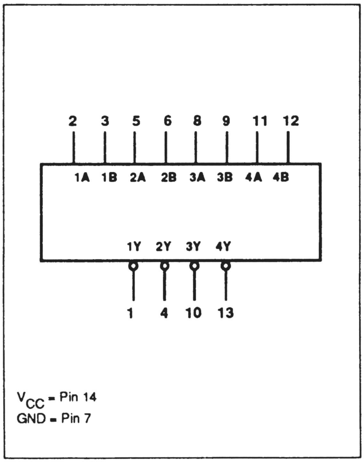
NOTE:
One (1.0) ALS Unit Load is defined as: 20μA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION



1$\overline{Y}$ 1
1A 2
1B 3
2$\overline{Y}$ 4
2A 5
2B 6
GND 7
14 V_{CC}
13 4$\overline{Y}$
12 4B
11 4A
10 3$\overline{Y}$
9 3B
8 3A

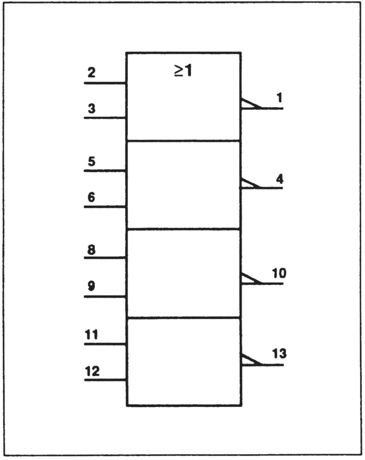
LOGIC SYMBOL



2 3 5 6 8 9 11 12
1A 1B 2A 2B 3A 3B 4A 4B
1Y 2Y 3Y 4Y
1 4 10 13

V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ± 10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}- 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 0V		0.86	2.2	mA
		I_{CCL}		V_I = 4.5V		2.16	4.0	mA

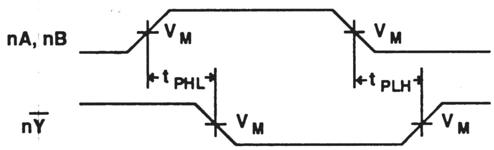
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA or nB to n$\overline{Y}$	Waveform 1	2.0 2.0	12.0 10.0	ns

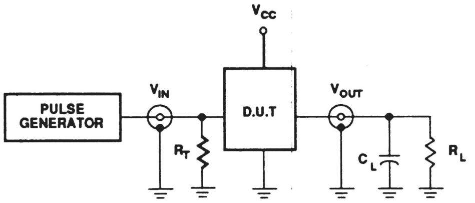
AC WAVEFORM


nA, nB
V_M
V_M
t_{PHL}
t_{PLH}
n$\overline{Y}$
V_M
V_M

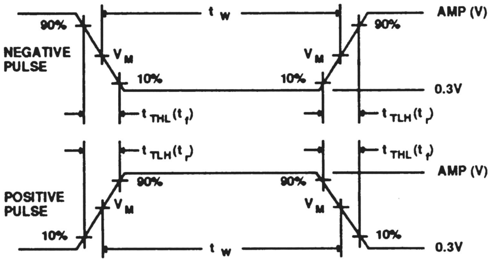
Waveform 1. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
V_{IN}
PULSE GENERATOR
D.U.T
V_{OUT}
R_T
C_L
R_L

Test Circuit for Totem-Pole Outputs


t_W
90%
90%
AMP (V)
NEGATIVE PULSE
V_M
V_M
10%
10%
0.3V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0.3V
t_W

V_M = 1.3V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS04B
Hex Inverters

Product Specification

FUNCTION TABLE

INPUT	OUTPUT
A	**$\overline{Y}$**
L	H
H	L

NOTES:
H = High voltage level
L = Low voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS04B	3.5 ns	2.0 mA

ORDERING INFORMATION

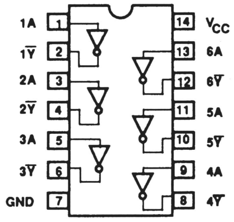
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74ALS04BN
14-Pin Plastic SO	74ALS04BD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

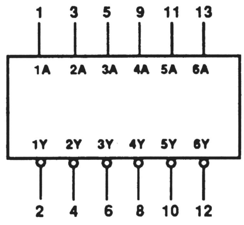
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA	Data input	1.0/1.0	20µA/0.1mA
n$\overline{Y}$	Data Output	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

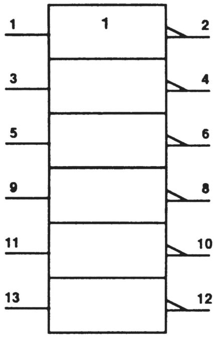

1A 1
1$\overline{Y}$ 2
2A 3
2$\overline{Y}$ 4
3A 5
3$\overline{Y}$ 6
GND 7
14 V_{CC}
13 6A
12 6$\overline{Y}$
11 5A
10 5$\overline{Y}$
9 4A
8 4$\overline{Y}$

LOGIC SYMBOL


1 3 5 9 11 13
1A 2A 3A 4A 5A 6A
1Y 2Y 3Y 4Y 5Y 6Y
2 4 6 8 10 12

V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)


1
1
2
3
4
5
6
9
8
11
10
13
12

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ± 10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}- 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 0V		0.75	1.1	mA
		I_{CCL}		V_I = 4.5V		3.2	4.2	mA

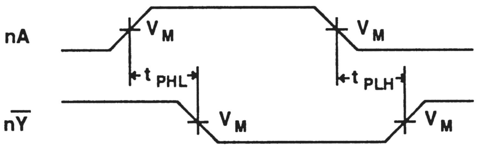
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA to n$\overline{Y}$	Waveform 1	2.0 2.0	11.0 8.0	ns

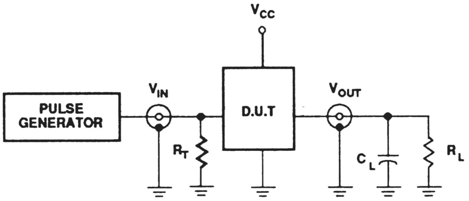
AC WAVEFORM


nA
V M
V M
t PHL
t PLH
n$\overline{Y}$
V M
V M

Waveform 1. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V CC
V IN
V OUT
PULSE GENERATOR
D.U.T
R T
C L
R L

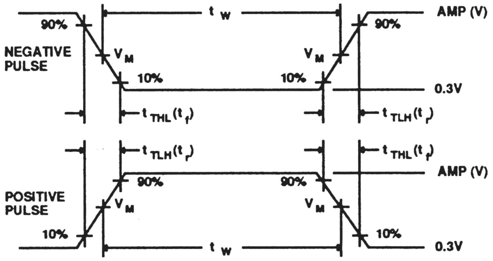
Test Circuit for Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t w
AMP (V)
90%
90%
NEGATIVE PULSE
V M
V M
10%
10%
0.3V
t THL (t f)
t TLH (t r)
t TLH (t r)
t THL (t f)
AMP (V)
90%
90%
POSITIVE PULSE
V M
V M
10%
10%
t w
0.3V

V_M = 1.3V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS08

Quad 2-Input AND Gates

Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	**Y**
H	H	H
L	X	L
X	L	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS08	5.0 ns	1.8 mA

ORDERING INFORMATION

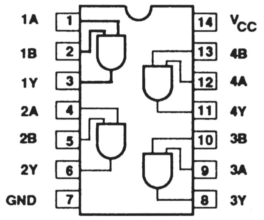
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74ALS08N
14-Pin Plastic SO	74ALS08D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

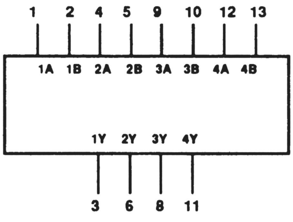
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB	Data inputs	1.0/1.0	20µA/0.1mA
nY	Data Output	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

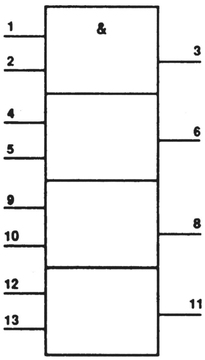

1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 V_{CC}
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y

LOGIC SYMBOL


1 2 4 5 9 10 12 13
1A 1B 2A 2B 3A 3B 4A 4B
1Y 2Y 3Y 4Y
3 6 8 11

V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)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November 4, 1986

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		$V_{CC} \pm 10\%$, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}- 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 4.5V		1.3	2.4	mA
		I_{CCL}		V_I = 0V		2.2	4.0	mA

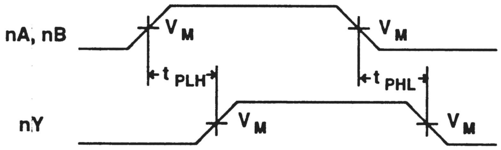
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA or nB to nY	Waveform 1	2.0 3.0	14.0 10.0	ns

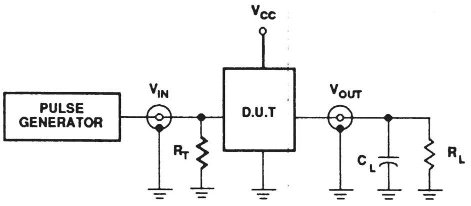
AC WAVEFORM


nA, nB
V_M
V_M
t_{PLH}
t_{PHL}
nY
V_M
V_M

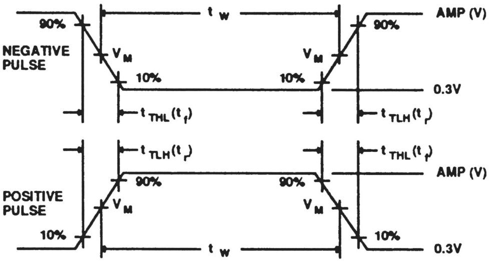
Waveform 1. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

Test Circuit for Totem-Pole Outputs


90%
NEGATIVE PULSE
V_M
10%
t_w
AMP (V)
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
POSITIVE PULSE

V_M = 1.3V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS10A

Triple 3-Input NAND Gates

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS10A	4.0 ns	1.0 mA

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	$\overline{Y}$
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

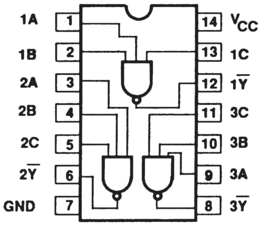
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V\pm10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	74ALS10AN
14-Pin Plastic SO	74ALS10AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

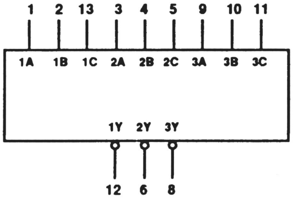
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB, nC	Data inputs	1.0/1.0	20µA/0.1mA
n$\overline{Y}$	Data Output	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

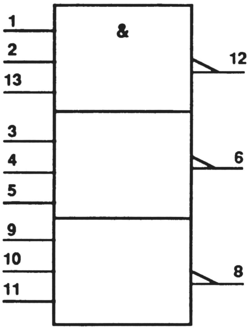

1A
1B
2A
2B
2C
2$\overline{Y}$
GND
V_{CC}
1C
1$\overline{Y}$
3C
3B
3A
3$\overline{Y}$
1
2
3
4
5
6
7
14
13
12
11
10
9
8

LOGIC SYMBOL


1
2
13
3
4
5
9
10
11
1A
1B
1C
2A
2B
2C
3A
3B
3C
1Y
2Y
3Y
12
6
8

V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)


&
1
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November 4, 1986

Triple 3-Input NAND Gates 74ALS10A

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		$V_{CC} \pm 10\%$, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}- 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 0V		0.5	0.6	mA
		I_{CCL}		V_I = 4.5V		1.6	2.2	mA

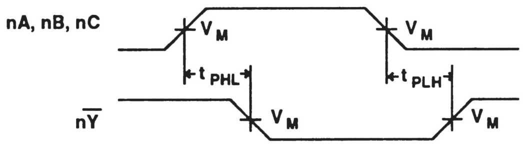
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to $n\overline{Y}$	Waveform 1	2.0 2.0	11.0 10.0	ns

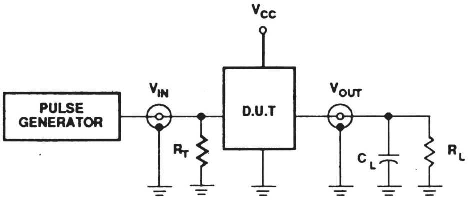
AC WAVEFORM


nA, nB, nC
V_M
V_M
t_{PHL}
t_{PLH}
$n\overline{Y}$
V_M
V_M

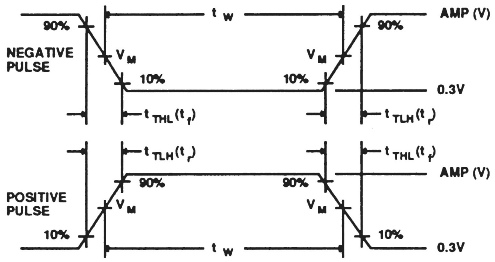
Waveform 1. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

Test Circuit for Totem-Pole Outputs


t_W
90%
AMP (V)
NEGATIVE PULSE
V_M
10%
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
POSITIVE PULSE
t_W

V_M = 1.3V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

74ALS11A

Triple 3-Input AND Gates

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS11A	5.5 ns	1.3 mA

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

NOTES:

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74ALS11AN
14-Pin Plastic SO	74ALS11AD

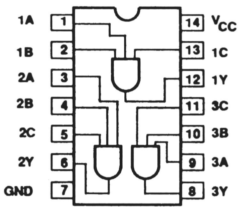
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB, nC	Data inputs	1.0/1.0	20µA/0.1mA
nY	Data Output	20/80	0.4mA/8mA

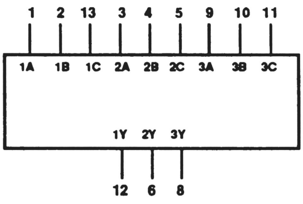
NOTE:

One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

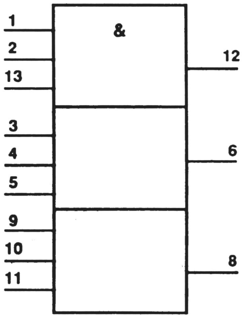

1A 1
1B 2
2A 3
2B 4
2C 5
2Y 6
GND 7
14 V_{CC}
13 1C
12 1Y
11 3C
10 3B
9 3A
8 3Y

LOGIC SYMBOL


1
2
13
3
4
5
9
10
11
1A
1B
1C
2A
2B
2C
3A
3B
3C
1Y
2Y
3Y
12
6
8

V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)


&
1
2
13
12
3
4
5
6
9
10
11
8

September 21, 1988

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		$V_{CC} \pm 10\%$, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		$V_{CC} - 2$			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 4.5V		1.0	1.8	mA
		I_{CCL}		V_I = 0V		2.0	3.0	mA

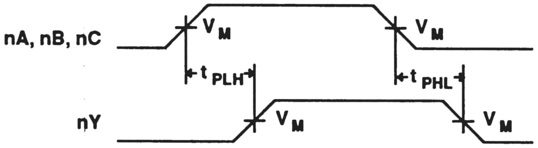
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to nY	Waveform 1	2.0 2.0	13.0 10.0	ns

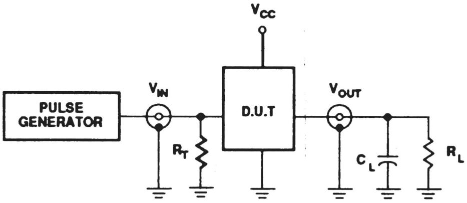
AC WAVEFORM


nA, nB, nC
V_M
V_M
t_{PLH}
t_{PHL}
nY
V_M
V_M

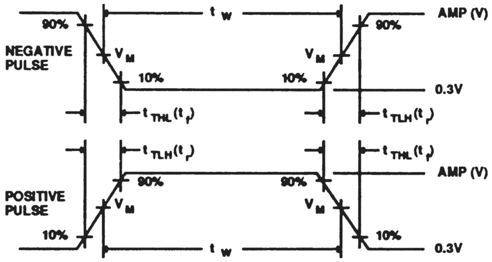
Waveform 1. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

Test Circuit for Totem-Pole Outputs


t_W
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
t_W
0.3V

V_M = 1.3V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

74ALS20A

Dual 4-Input NAND Gates

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS20A	4.5 ns	0.65 mA

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	$\overline{Y}$
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

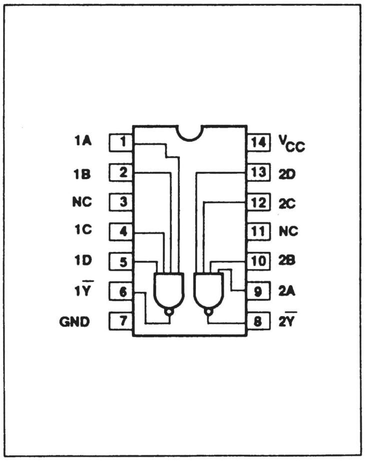
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74ALS20AN
14-Pin Plastic SO	74ALS20AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

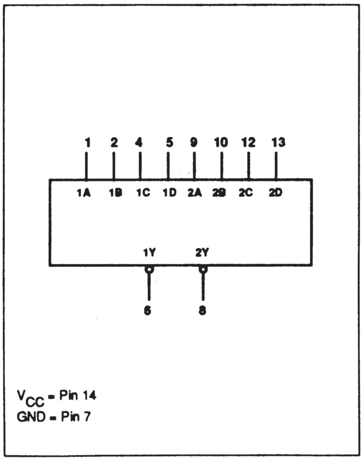
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB, nC, nD	Data inputs	1.0/1.0	20μA/0.1mA
n$\overline{Y}$	Data Output	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20μA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

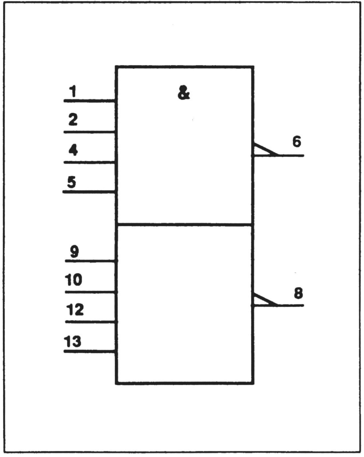

1A
1B
NC
1C
1D
1$\overline{Y}$
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V_{CC}
2D
2C
NC
2B
2A
2$\overline{Y}$

LOGIC SYMBOL


1
2
4
5
9
10
12
13
1A
1B
1C
1D
2A
2B
2C
2D
1Y
2Y
6
8

V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)


&
1
2
4
5
6
9
10
12
13
8

November 4, 1986

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ± 10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}- 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 0V		0.3	0.4	mA
		I_{CCL}		V_I = 4.5V		1.0	1.5	mA

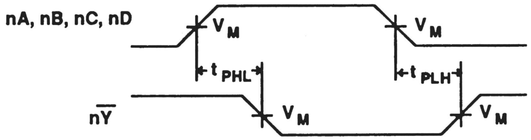
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to $n\overline{Y}$	Waveform 1	2.0 3.0	11.0 10.0	ns

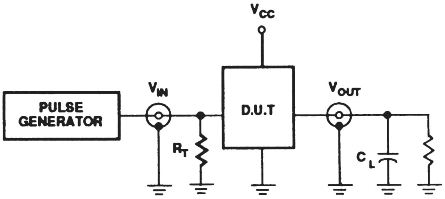
AC WAVEFORM


nA, nB, nC, nD
V_M
V_M
t_{PHL}
t_{PLH}
$n\overline{Y}$
V_M
V_M

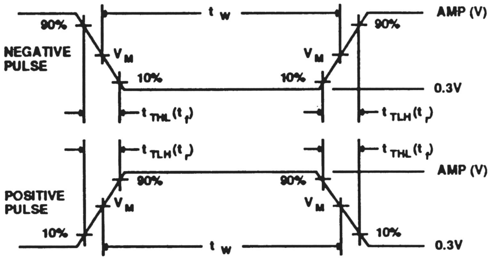
Waveform 1. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
V_{IN}
PULSE GENERATOR
D.U.T
V_{OUT}
R_T
C_L
R_L

Test Circuit for Totem-Pole Outputs


90%
NEGATIVE PULSE
V_M
10%
t_W
AMP (V)
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
POSITIVE PULSE

V_M = 1.3V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS27

Triple 3-Input NOR Gates

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS27	4.0 ns	1.5 mA

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	$\overline{Y}$
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

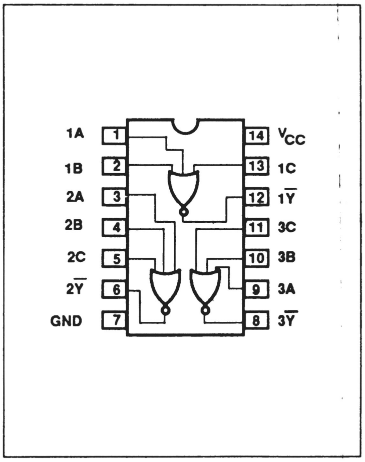
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74ALS27N
14-Pin Plastic SO	74ALS27D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

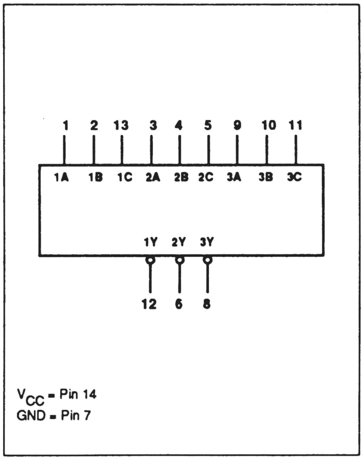
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB, nC	Data inputs	1.0/1.0	20µA/0.1mA
n$\overline{Y}$	Data Output	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

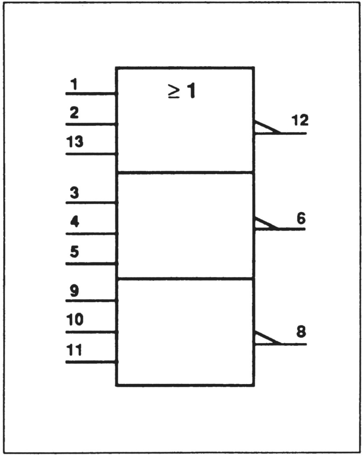

1A 1
1B 2
2A 3
2B 4
2C 5
2$\overline{Y}$ 6
GND 7
14 V_{CC}
13 1C
12 1$\overline{Y}$
11 3C
10 3B
9 3A
8 3$\overline{Y}$

LOGIC SYMBOL


1 2 13 3 4 5 9 10 11
1A 1B 1C 2A 2B 2C 3A 3B 3C
1Y 2Y 3Y
12 6 8

V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)


≥1
1
2
13
12
3
4
5
6
9
10
11
8

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	**Nom**	**Max**	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	**Typ[2]**	**Max**	
V_{OH}	High-level output voltage		V_{CC} ± 10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}- 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 0V		1.0	1.8	mA
		I_{CCL}		V_I = 4.5V		2.0	4.0	mA

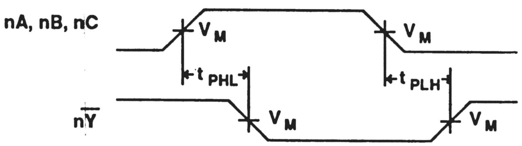
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	Waveform 1	2.0 2.0	15.0 9.0	ns

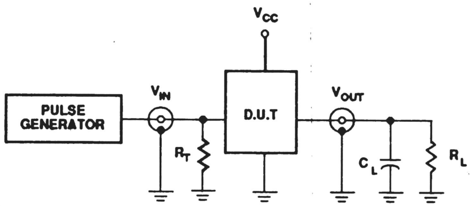
AC WAVEFORM


nA, nB, nC
V_M
V_M
t_{PHL}
t_{PLH}
n$\overline{Y}$
V_M
V_M

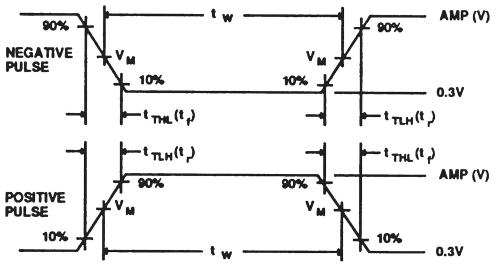
Waveform 1. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_T
C_L
R_L

Test Circuit for Totem-Pole Outputs


90%
NEGATIVE PULSE
V_M
10%
t_W
AMP (V)
90%
V_M
10%
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
t_W
0.3V

V_M = 1.3V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS30A

8-Input NAND Gate

Preliminary Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS30A	7.0 ns	0.5 mA

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	$\overline{Y}$
H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H

NOTES:

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

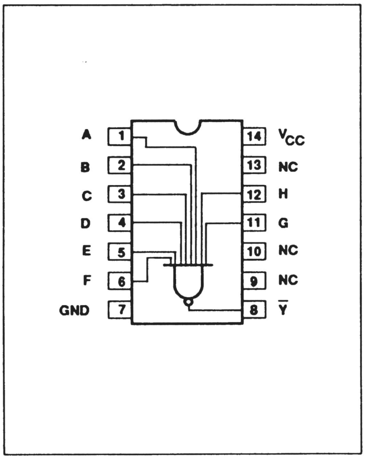
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74ALS30AN
14-Pin Plastic SO	74ALS30AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

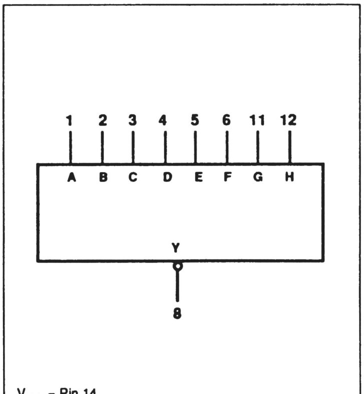
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A - H	Data inputs	1.0/1.0	20μA/0.1mA
$\overline{Y}$	Data Output	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20μA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

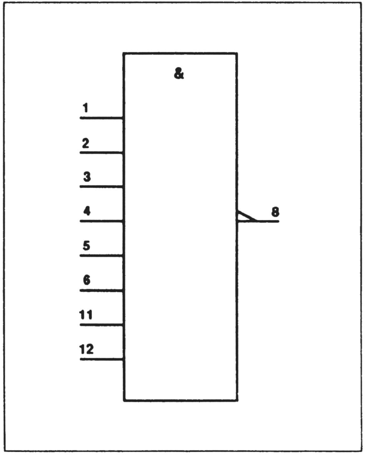

A
1
B
2
C
3
D
4
E
5
F
6
GND
7
14
V_{CC}
13
NC
12
H
11
G
10
NC
9
NC
8
$\overline{Y}$

LOGIC SYMBOL


1
2
3
4
5
6
11
12
A
B
C
D
E
F
G
H
Y
8

V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)


&
1
2
3
4
5
6
11
12
8

March 1988

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ± 10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}- 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 0V		0.22	0.36	mA
		I_{CCL}		V_I = 4.5V		0.54	0.9	mA

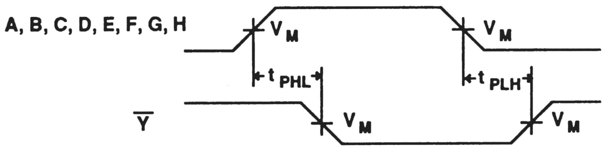
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay A,B,C,D,E,F,G,H to $\overline{Y}$	Waveform 1	3.0 3.0	10.0 12.0	ns

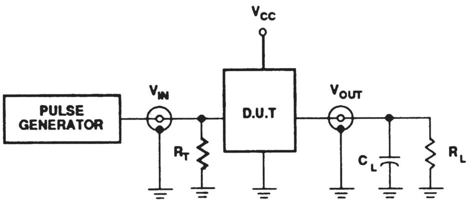
AC WAVEFORM


A, B, C, D, E, F, G, H
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}$
V_M
V_M

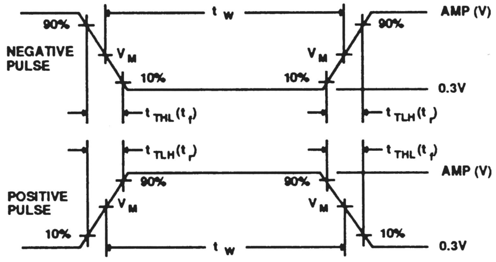
Waveform 1. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_T
C_L
R_L

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
V_M
10%
t_w
90%
V_M
10%
AMP (V)
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
POSITIVE PULSE
90%
V_M
10%
90%
V_M
10%
t_w
AMP (V)
0.3V

V_M = 1.3V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

74ALS32

Quad 2-Input OR Gates

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS32	5.0 ns	2.3 mA

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

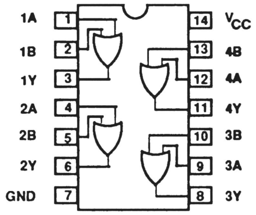
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74ALS32N
14-Pin Plastic SO	74ALS32D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

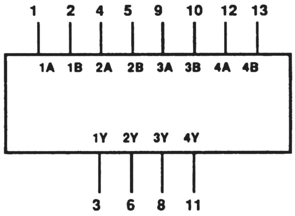
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB	Data inputs	1.0/1.0	20µA/0.1mA
nY	Data Output	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

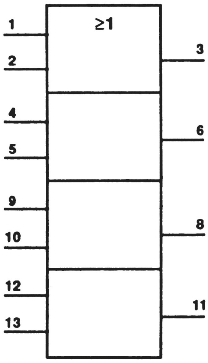

1A
1
1B
2
1Y
3
2A
4
2B
5
2Y
6
GND
7
14
VCC
13
4B
12
4A
11
4Y
10
3B
9
3A
8
3Y

LOGIC SYMBOL


1
2
4
5
9
10
12
13
1A
1B
2A
2B
3A
3B
4A
4B
1Y
2Y
3Y
4Y
3
6
8
11

V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)


≥1
1
2
3
4
5
6
9
10
8
12
13
11

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$V_{CC} \pm 10\%$, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}- 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	V_I = 4.5V		1.6	4.0	mA
	I_{CCL}		V_I = 0V		2.8	4.9	mA

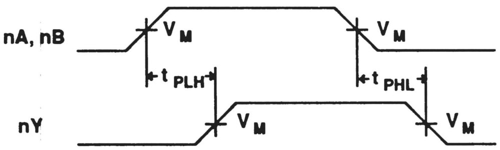
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA or nB to nY	Waveform 1	2.0 3.0	14.0 12.0	ns

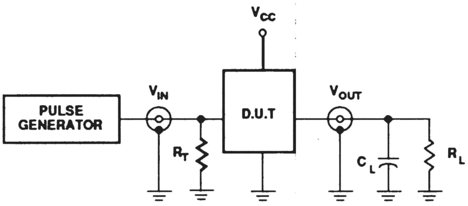
AC WAVEFORM


nA, nB
V_M
V_M
t_{PLH}
t_{PHL}
nY
V_M
V_M

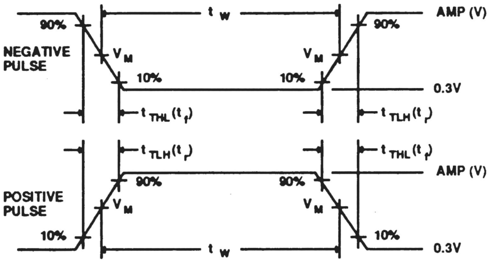
Waveform 1. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_w
t_{THL} (t_f)
t_{TLH} (t_r)
AMP (V)
0.3V

V_M = 1.3V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS38A

Buffer

Quad Two-Input NAND Buffer (Open-Collector)
Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	**$\overline{Y}$**
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS38A	7.0 ns	3.5 mA

ORDERING INFORMATION

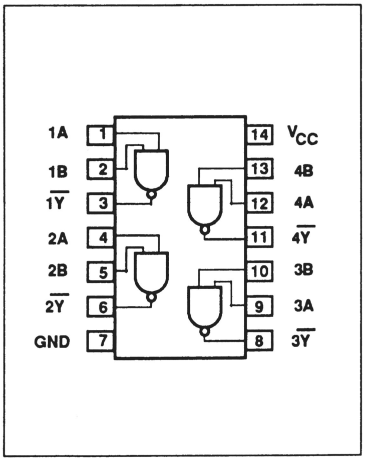
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74ALS38AN
14-Pin Plastic SO	74ALS38AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

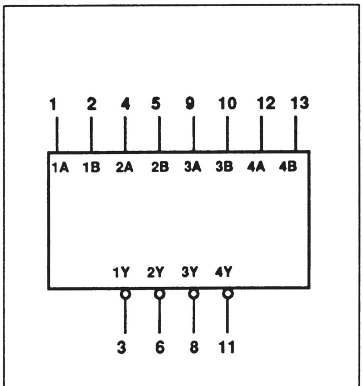
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20µA/0.1mA
$\overline{Y}$	Outputs	*OC/1.0	*OC/24mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.
*OC = Open Collector

PIN CONFIGURATION

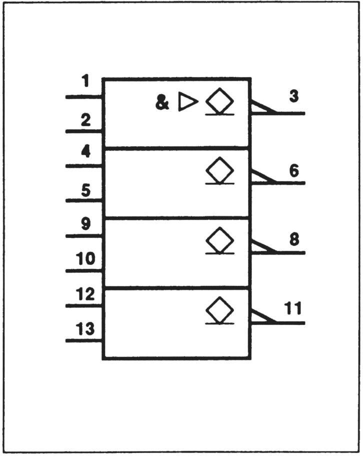

1A
1B
$\overline{1Y}$
2A
2B
$\overline{2Y}$
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V_{CC}
4B
4A
$\overline{4Y}$
3B
3A
$\overline{3Y}$

LOGIC SYMBOL


1
2
4
5
9
10
12
13
1A
1B
2A
2B
3A
3B
4A
4B
1Y
2Y
3Y
4Y
3
6
8
11

V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL(IEEE/IEC)


1
2
4
5
9
10
12
13
&
3
6
8
11

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC}= MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				100	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	I_{OL} = 12mA		0.25	0.4	V
			V_{IH} = MIN	I_{OL} = 24mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		0.65	1.6	mA
		I_{CCL}		V_{IN} = 4.5V		6.5	9.0	mA

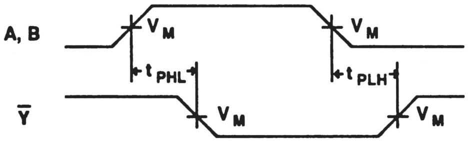
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	3.0 3.0	11 11	ns

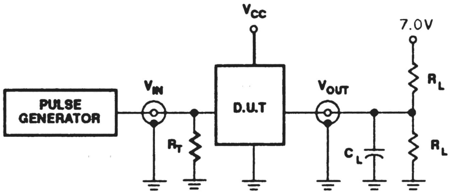
AC WAVEFORM


A, B
$\overline{Y}$
V_M
V_M
t_{PHL}
t_{PLH}
V_M
V_M

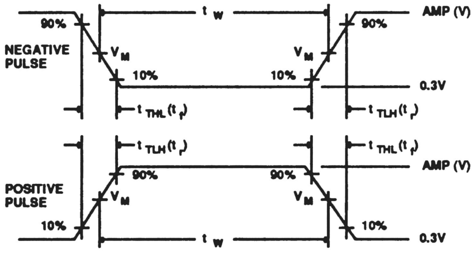
Waveform 1. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_L
R_T
C_L
R_L

Test Circuit for Open-Collector Outputs


t_W
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0.3V
t_W

V_M = 1.3V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

74ALS74A
FLIP-FLOP

74ALS74A Dual D-Type Flip-Flops with Set and Reset

Product Specification

DESCRIPTION

The 'ALS74A is a dual edge-triggered D-type flip-flop featuring individual data, Set and Reset inputs, with true and complementary outputs. Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are synchronous active-Low inputs and operate independently of the Clock (CP) input. When $\overline{S}_D$ and $\overline{R}_D$ are inactive (High), data at the D input is transferred to the Q and $\overline{Q}$ outputs on the Low-to-High transition of the CP. Data must be stable one setup time prior to the Low-to-High clock transition for predictable operation. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS74A	150 MHz	3.0mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74ALS74AN
14-Pin Plastic SO	N74ALS74AD

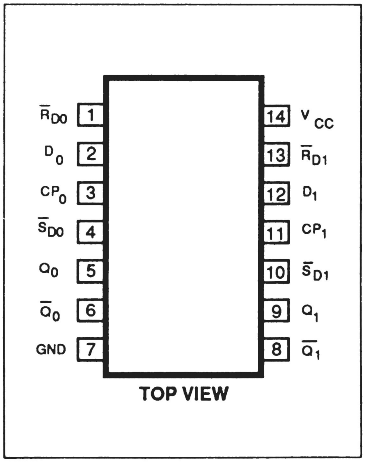
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/2.0	20µA/0.2mA
CP_0, CP_1	Clock inputs (Acting rising edge)	1.0/2.0	20µA/0.2mA
$\overline{S}_{D0}, \overline{S}_{D1}$	Set inputs (Active Low)	2.0/4.0	40µA/0.4mA
$\overline{R}_{D0}, \overline{R}_{D1}$	Reset inputs (Active Low)	2.0/4.0	40µA/0.4mA
$Q_0, Q_1, \overline{Q}_0, \overline{Q}_1$	Data outputs	20/80	0.4mA/8mA

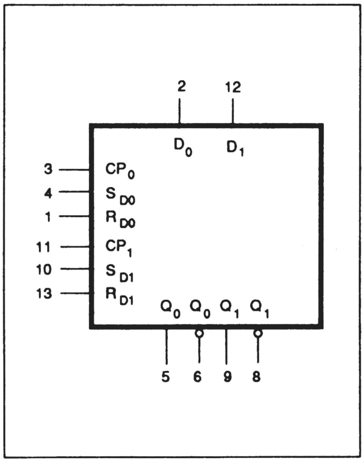
NOTE:

One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

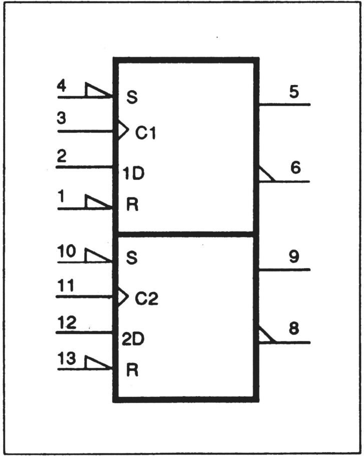
PIN CONFIGURATION


$\overline{R}_{D0}$ 1
D_0 2
CP_0 3
$\overline{S}_{D0}$ 4
Q_0 5
$\overline{Q}_0$ 6
GND 7
$\overline{Q}_1$ 8
Q_1 9
$\overline{S}_{D1}$ 10
CP_1 11
D_1 12
$\overline{R}_{D1}$ 13
V_{CC} 14
TOP VIEW

LOGIC SYMBOL

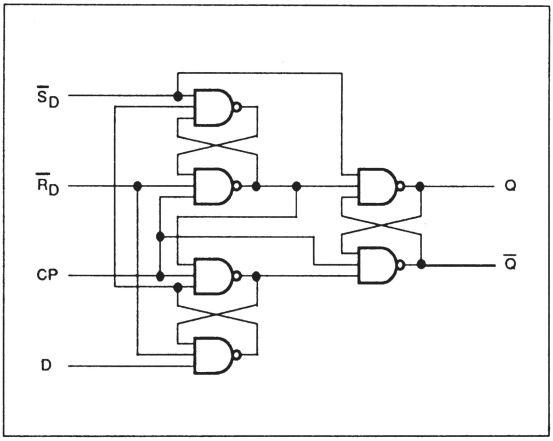

2
12
D_0
D_1
3 CP_0
4 S_{D0}
1 R_{D0}
11 CP_1
10 S_{D1}
13 R_{D1}
Q_0
Q_0
Q_1
Q_1
5
6
9
8

LOGIC SYMBOL(IEEE/IEC)


4 S
3 C1
2 1D
1 R
5
6
10 S
11 C2
12 2D
13 R
9
8

October 8, 1987

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Reset
L	L	X	X	H*	H*	Undetermined *
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	L	X	NC	NC	Hold

H = High voltage level
h-= High voltage level one setup time prior to Low-toHigh clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
NC=No change from the previous setup
X = Don't care
↑ = Low-to-High clock transition
* =Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	V_{CC}-2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.5	V
I_I	Input current at maximum input voltage	D_n, CP_n	V_{CC} = MAX, V_I = 7.0V				0.1	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					0.2	mA
I_{IH}	High-level input current	D_n, CP_n	V_{CC} = MAX, V_I = 2.7V				20	μA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$			-120		-40	μA
I_{IL}	Low-level input current	D_n, CP_n	V_{CC} = MAX, V_I = 0.4V				-0.2	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					-0.4	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			3.0	4.0	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
4. Measure I_{CC} with the D_n, CP_n, and $\overline{S}_{Dn}$ grounded, then with D_n, CP_n, and $\overline{R}_{Dn}$ grounded.

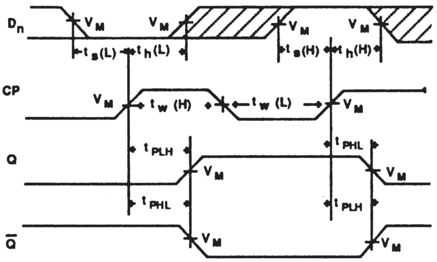
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74ALS74A		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2, 3	1.0 3.0	8.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	3.0 3.0	14.0 14.0	ns

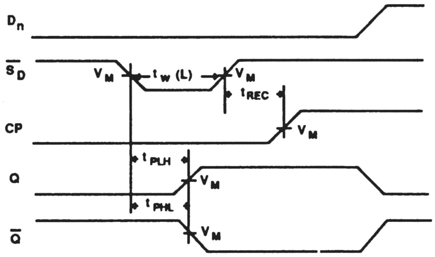
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74ALS74A		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 1	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 1	0 0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width, High or Low	Waveform 1	6.0 6.0		ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ pulse width, Low	Waveform 2, 3	6.0		ns
t_{rec}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP	Waveform 2, 3	6.0		ns

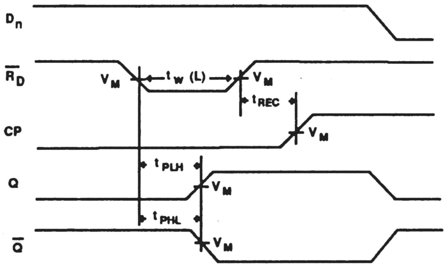
AC WAVEFORMS


D_n
V_M
t_s(L)
t_h(L)
t_s(H)
t_h(H)
CP
t_w(H)
t_w(L)
Q
t_PLH
t_PHL
Q̄

Waveform 1. Propagation delay for data to output, data setup time and hold times and clock width


D_n
S̄_D
V_M
t_w(L)
t_REC
CP
Q
t_PLH
t_PHL
Q̄

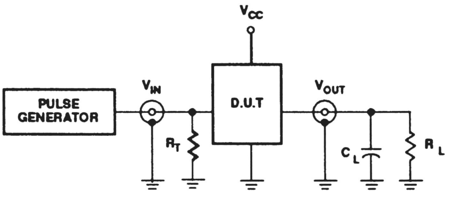
Waveform 2. Propagation delay for set to output, set pulse width and recovery time for set to clock


D_n
R̄_D
V_M
t_w(L)
t_REC
CP
Q
t_PLH
t_PHL
Q̄

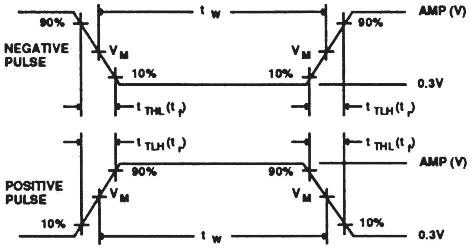
Waveform 3. Propagation delay for reset to output, reset pulse width and recovery time for reset to clock

NOTE: For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
R_T
D.U.T
V_OUT
C_L
R_L

Test Circuit For Totem-Pole Outputs


t_w
90%
AMP (V)
NEGATIVE PULSE
V_M
10%
0.3V
t_THL(t_f)
t_TLH(t_r)
POSITIVE PULSE

V_M = 1.3V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

74ALS86

Quad 2-Input Exclusive-OR Gates

Product Specification

DESCRIPTION

These devices contain four independent 2-input Exclusive-OR gates. A common application is a true/complement element. If one input is held Low, the signal on the other input will be reproduced in true form at the output. If one input is held High, the signal on the other input will be reproduced inverted at the output.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

NOTES:
H = High voltage level
L = Low voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS86	6.0 ns	3.9 mA

ORDERING INFORMATION

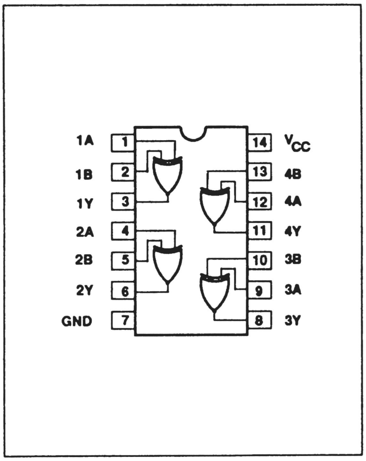
PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	74ALS86N
14-Pin Plastic SO	74ALS86D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

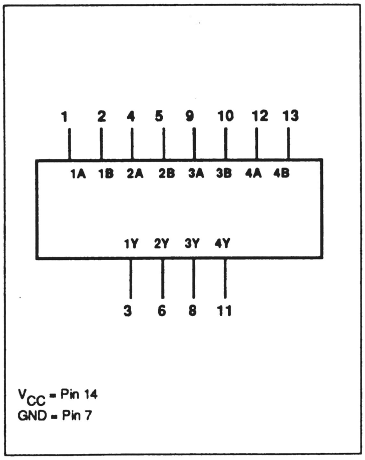
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB	Data inputs	1.0/1.0	20µA/0.1mA
nY	Data Output	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

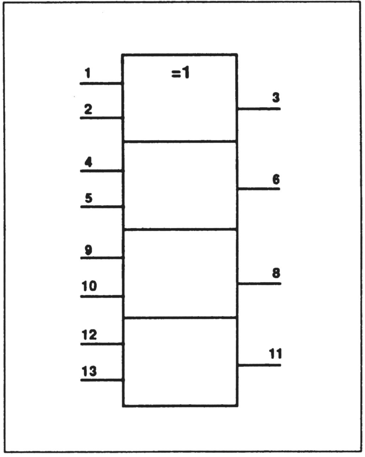
PIN CONFIGURATION


1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y

LOGIC SYMBOL


1 2 4 5 9 10 12 13
1A 1B 2A 2B 3A 3B 4A 4B
1Y 2Y 3Y 4Y
3 6 8 11
VCC = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)


=1
1
2
3
4
5
6
9
10
8
12
13
11

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} ± 10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}- 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, V_I = 4.5V			3.9	5.9	mA

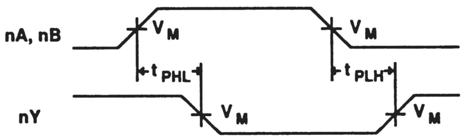
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

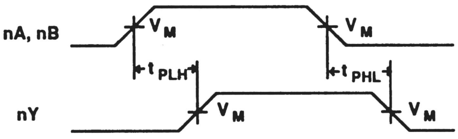
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% R_L = 500Ω C_L = 50pF		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA or nB to nY	Waveform 2 (other input Low)	2.0 2.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay nA or nB to nY	Waveform 1 (other input High)	2.0 2.0	12.0 12.0	ns

AC WAVEFORM


nA, nB
V_M
V_M
t_{PHL}
t_{PLH}
nY
V_M
V_M

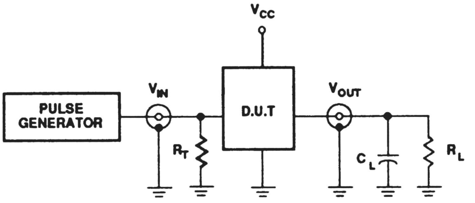
Waveform 1. Propagation Delay for Data to Output


nA, nB
V_M
V_M
t_{PLH}
t_{PHL}
nY
V_M
V_M

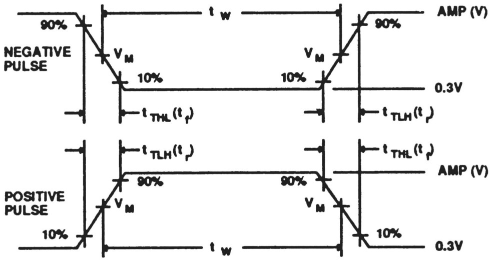
Waveform 2. Propagation Delay for Data to Output

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
V_M
10%
t_w
V_M
10%
90%
AMP (V)
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
POSITIVE PULSE
t_{TLH} (t_r)
t_{THL} (t_f)
90%
V_M
10%
90%
V_M
10%
AMP (V)
0.3V
t_w

V_M = 1.3V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

74ALS109A

FLIP-FLOP

74ALS109A Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops With Set and Reset

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS109A	150 MHz	3.0mA

DESCRIPTION

The 'ALS109A is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock (CP) input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Mode Select Function Table.

The J and $\overline{K}$ inputs must be stable just one setup time prior to the Low-to-High transition of the clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying J and $\overline{K}$ inputs together.

Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

ORDERING INFORMATION

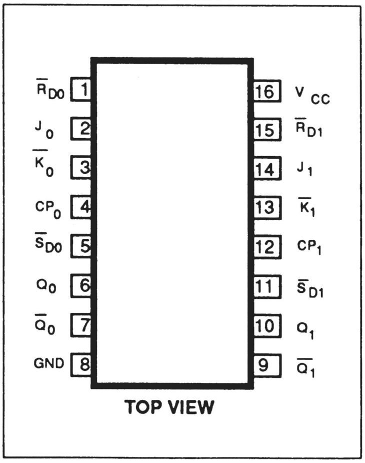
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	74ALS109AN
16-Pin Plastic SO	74ALS109AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

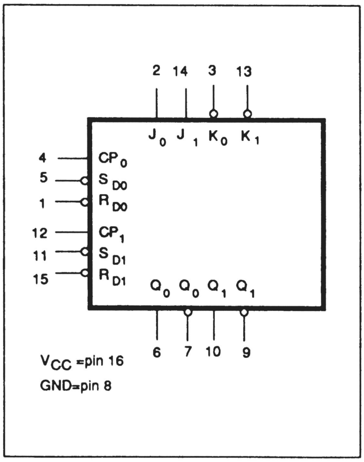
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/2.0	20µA/0.2mA
$\overline{K}_0$, $\overline{K}_1$	K inputs	1.0/2.0	20µA/0.2mA
CP_0, CP_1	Clock inputs (Acting rising edge)	1.0/2.0	20µA/0.2mA
$\overline{S}_{D0}$, $\overline{S}_{DI}$	Set inputs (Active Low)	1.0/4.0	20µA/0.4mA
$\overline{R}_{D0}$, $\overline{R}_{DI}$	Reset inputs (Active Low)	1.0/4.0	20µA/0.4mA
Q_0, Q_I, $\overline{Q}_0$, $\overline{Q}_I$	Data outputs	20/80	0.4mA/6mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

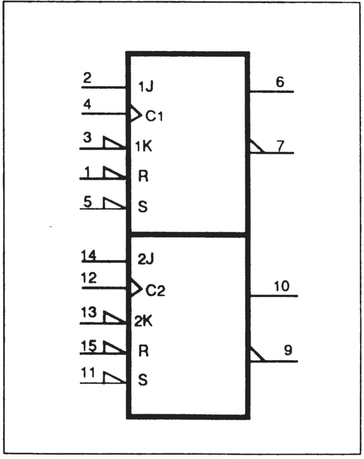
PIN CONFIGURATION


$\overline{R}_{D0}$ 1
J_0 2
$\overline{K}_0$ 3
CP_0 4
$\overline{S}_{D0}$ 5
Q_0 6
$\overline{Q}_0$ 7
GND 8
16 V_{CC}
15 $\overline{R}_{D1}$
14 J_1
13 $\overline{K}_1$
12 CP_1
11 $\overline{S}_{D1}$
10 Q_1
9 $\overline{Q}_1$
TOP VIEW

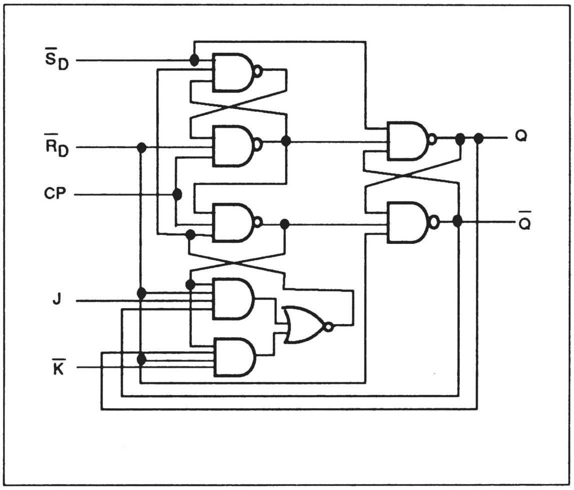
LOGIC SYMBOL


2 14 3 13
J_0 J_1 K_0 K_1
4 CP_0
5 S_{D0}
1 R_{D0}
12 CP_1
11 S_{D1}
15 R_{D1}
Q_0 Q_0 Q_1 Q_1
6 7 10 9
V_{CC} =pin 16
GND=pin 8

LOGIC SYMBOL(IEEE/IEC)


2 1J
4 C1
3 1K
1 R
5 S
6
7
14 2J
12 C2
13 2K
15 R
11 S
10
9

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H*	H*	Undetermined*
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	l	l	L	H	Load "0"
H	H	↑	h	h	H	L	Load "1"
H	H	↑	L	h	q	$\overline{q}$	Hold "no change"
H	H	L	X	X	q	$\overline{q}$	Hold "no change"

H = High voltage level
h-= High voltage level one setup time prior to Low-toHigh clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
NC=No change from the previous setup
X = Don't care
↑ = Low-to-High clock transition
* =The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the Set and Reset are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not remain when either Set or Reset returns to its inactive (High) level.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	V_{CC}-2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.5	V
I_I	Input current at maximum input voltage	J, $\overline{K}$, CP_n	V_{CC} = MAX, V_I = 7.0V				0.1	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					0.2	mA
I_{IH}	High-level input current	J, $\overline{K}$, CP_n	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$			-120		-40	µA
I_{IL}	Low-level input current	J, $\overline{K}$, CP_n	V_{CC} = MAX, V_I = 0.4V				-0.2	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					-0.4	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			3.0	4.0	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

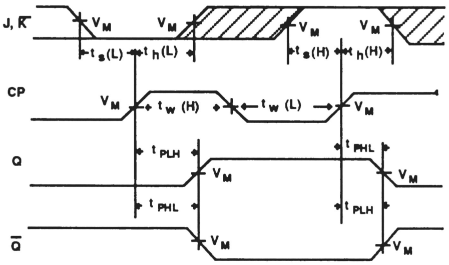
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74ALS109A		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2, 3	1.0 3.0	8.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	3.0 3.0	14.0 14.0	ns

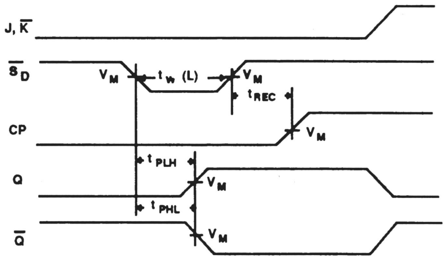
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74ALS109A		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Max	
t_s(H) t_s(L)	Setup time, High or Low J, $\overline{K}$ to CP	Waveform 1	6.0 6.0		ns
t_h(H) t_h(L)	Hold time, High or Low J, $\overline{K}$ to CP	Waveform 1	0 0		ns
t_w(H) t_w(L)	Clock pulse width, High or Low	Waveform 1	6.0 6.0		ns
t_w(H)	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ pulse width, Low	Waveform 2, 3	6.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP	Waveform 2, 3	6.0		ns

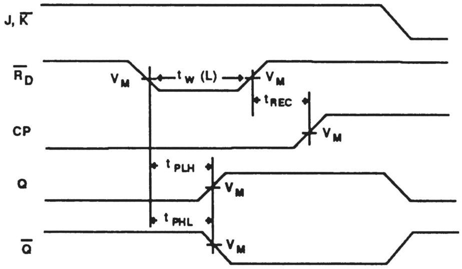
AC WAVEFORMS


J, K̄
V_M
t_s(L)
t_h(L)
t_s(H)
t_h(H)
CP
t_w (H)
t_w (L)
Q
t_PLH
t_PHL
Q̄

Waveform 1. Propagation delay for data to output, data setup time and hold times and clock width


J, K̄
S̄_D
V_M
t_w (L)
t_REC
CP
Q
t_PLH
t_PHL
Q̄

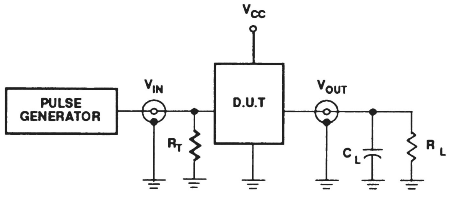
Waveform 2. Propagation delay for set to output, set pulse width and recovery time for set to clock


J, K̄
R̄_D
V_M
t_w (L)
t_REC
CP
Q
t_PLH
t_PHL
Q̄

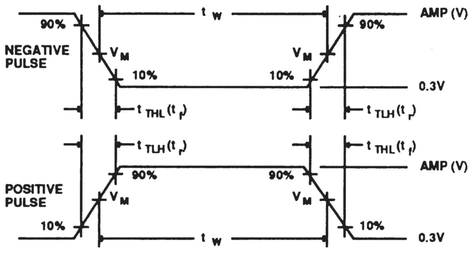
Waveform 3. Propagation delay for reset to output, reset pulse width and recovery time for reset to clock

NOTE: For all waveforms, $V_M = 1.3V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
D.U.T
V_OUT
R_T
C_L
R_L

Test Circuit For Totem-Pole Outputs


t_w
AMP (V)
90%
NEGATIVE PULSE
V_M
10%
0.3V
t_THL (t_f)
t_TLH (t_r)
POSITIVE PULSE

$V_M = 1.3V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS112A
Flip-Flop

Dual J-K Negative Edge-triggered Flip-Flop
Preliminary Specification

DESCRIPTION

The 74ALS112A, Dual Negative Edge-Triggered JK-Type Flip-Flop, features individual J, K, Clock ($\overline{CP}_n$), Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, true (Q_n) and complementary ($\overline{Q}_n$) outputs.

The $\overline{S}_D$ and $\overline{R}_D$ inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the level at the other inputs.

A High level on the clock ($\overline{CP}_n$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}_n$ is High and the flip-flop will perform according to the FunctionTable as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the $\overline{CP}_n$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS112A	50MHz	2.5mA

ORDERING INFORMATION

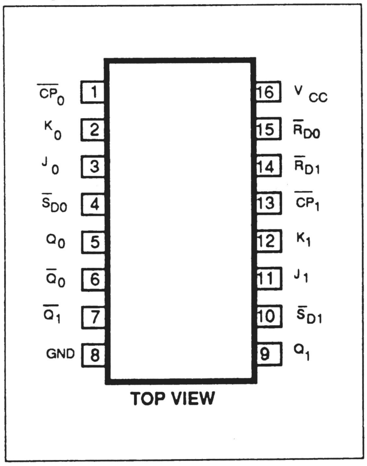
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74ALS112AN
16-Pin Plastic SO	N74ALS112AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

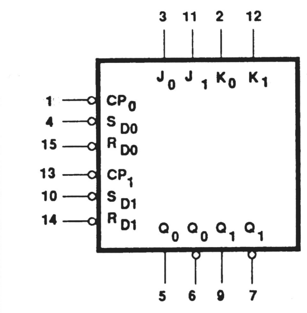
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/2.0	20µA/0.2mA
K_0, K_1	K inputs	1.0/2.0	20µA/0.2mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (Active Low)	2.0/4.0	40µA/0.4mA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (Active Low)	2.0/4.0	40µA/0.4mA
$\overline{CP}_0$, $\overline{CP}_1$	Clock Pulse input (Active falling edge)	1.0/2.0	20µA/0.2mA
Q_0,$\overline{Q}_0$; Q_1,$\overline{Q}_1$	Data outputs	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

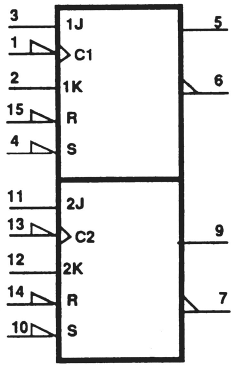

$\overline{CP}_0$ 1
K_0 2
J_0 3
$\overline{S}_{D0}$ 4
Q_0 5
$\overline{Q}_0$ 6
$\overline{Q}_1$ 7
GND 8
16 V_{CC}
15 $\overline{R}_{D0}$
14 $\overline{R}_{D1}$
13 $\overline{CP}_1$
12 K_1
11 J_1
10 $\overline{S}_{D1}$
9 Q_1
TOP VIEW

LOGIC SYMBOL


3
11
2
12
J_0
J_1
K_0
K_1
1
4
15
13
10
14
CP_0
S_{D0}
R_{D0}
CP_1
S_{D1}
R_{D1}
Q_0
Q_0
Q_1
Q_1
5
6
9
7

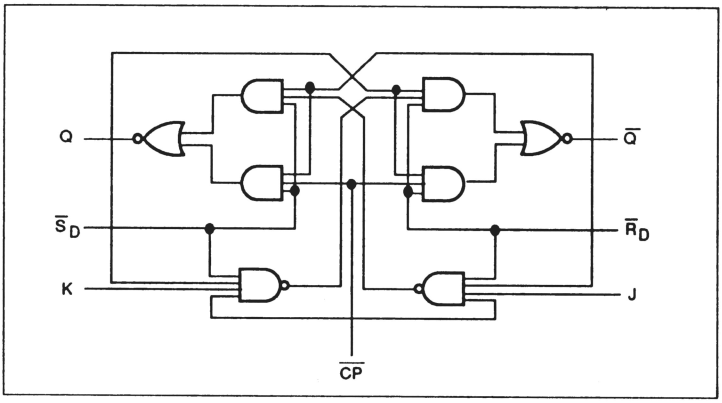
V_{CC}=pin 16
GND=pin 8

LOGIC SYMBOL(IEEE/IEC)


3
1J
1
C1
2
1K
15
R
4
S
5
6
11
2J
13
C2
12
2K
14
R
10
S
9
7

July 1988

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronmous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H*	H*	Undetermined *
H	H	↓	h	h	$\overline{q}$	q	Toggle
H	H	↓	l	h	L	H	Load "0"(Reset)
H	H	↓	h	l	H	L	Load "1" (Set)
H	H	↓	l	l	q	$\overline{q}$	Hold "no change"
H	H	H	X	X	q	$\overline{q}$	Hold "no change"

H = High voltage level
h-= High voltage level one setup time prior to High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to High-to-Low clock transition
q=Lower case letters indicate the state of the referenced output prior to the High-to-Low clock transition
X = Don't care
↓= High-to-Low clock transition
Asynchronous inputs: Low input to $\overline{S}_D$ sets Q to High level, Low input to $\overline{R}_D$ sets Q to Low level
Set and Reset are independent of clock
Simultaneous Low on both $\overline{S}_D$ and $\overline{R}_D$ makes both Q and $\overline{Q}$ High
* =Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -0.4mA		V_{CC}-2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.5	V
I_I	Input current at maximum input voltage	J_n, K_n, $\overline{CP}_n$	V_{CC} = MAX, V_I = 7.0V				100	µA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					200	µA
I_{IH}	High-level input current	J_n, K_n, $\overline{CP}_n$	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					40	µA
I_{IL}	Low-level input current	J_n, K_n, $\overline{CP}_n$	V_{CC} = MAX, V_I = 0.4V				-0.2	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					-0.4	mA
I_O[3]	Output current		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			2.5	4.5	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{os}.

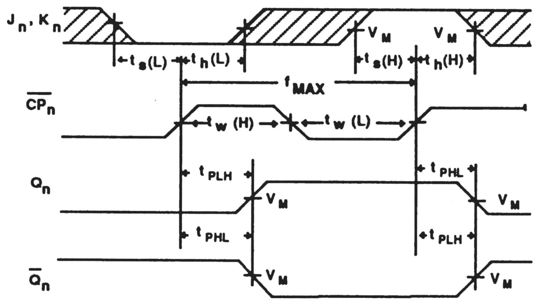
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	Waveform 1	3 5	15 19	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_D$ to Q_n or $\overline{Q}_n$	Waveform 2,3	3 4	15 18	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, K_n to $\overline{CP}_n$	Waveform 1	22 22		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, K_n to $\overline{CP}_n$	Waveform 1	0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ Pulse width, High or Low	Waveform 1	16.5 16.5		ns
$t_w(L)$	$\overline{S}_D$ or $\overline{R}_D$ Pulse width, Low	Waveform 2,3	10		ns
t_{rec}	Recovery time $\overline{S}_D$ or $\overline{R}_D$ to $\overline{CP}_n$	Waveform 2,3	20		ns

AC WAVEFORMS

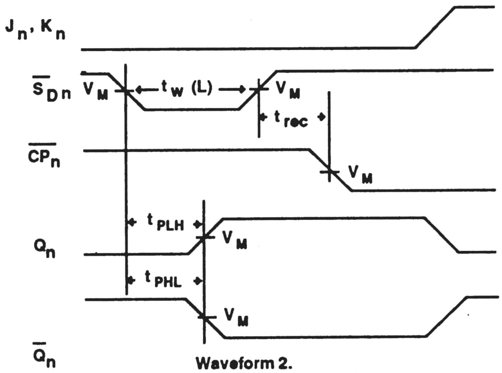


Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width

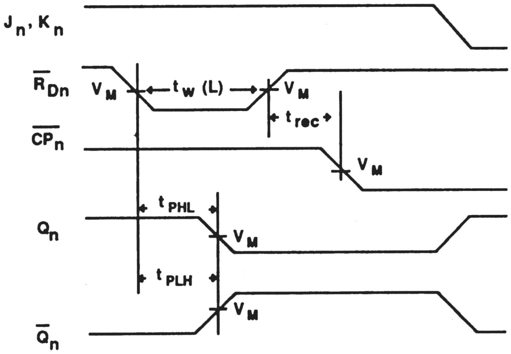
The shaded area indicate when the input is permitted to change for predictable output performance.

NOTE: For all waveforms, V_M = 1.3V.

AC WAVEFORMS


Jn, Kn
S̄Dn
VM
tw (L)
VM
trec
C̄P̄n
VM
tPLH
Qn
VM
tPHL
VM
Q̄n

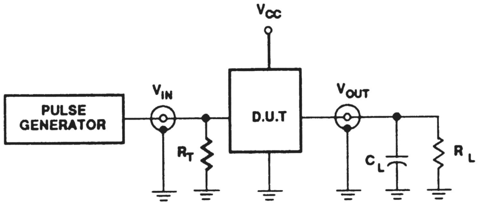
Waveform 2.
Propagation Delay for set to output, set pulse width, and recovery time for set to clock


Jn, Kn
R̄Dn
VM
tw (L)
VM
trec
C̄P̄n
VM
tPHL
Qn
VM
tPLH
VM
Q̄n

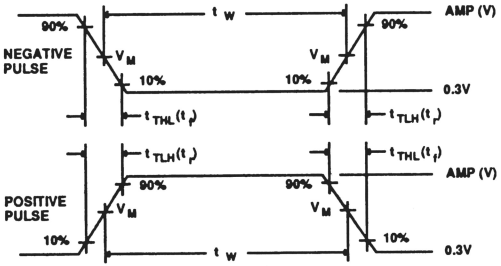
Waveform 3.
Propagation Delay for reset to output, reset pulse width, and recovery time for reset to clock

NOTE: For all waveforms, $V_M = 1.3V$.

TEST CIRCUIT AND WAVEFORMS


VCC
VIN
VOUT
PULSE GENERATOR
D.U.T
RT
CL
RL

Test Circuit For Totem-Pole Outputs


tw
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0.3V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
tw
0.3V

$V_M = 1.3V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS138
Decoder/Demultiplexer

1-Of-8 Decoder//Demultiplexer

Preliminary Specification

FEATURES
- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS138	12ns	5mA

DESCRIPTION

The 74ALS138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active-Low outputs ($\overline{Q}_0$-$\overline{Q}_7$). The device features three Enable inputs; two active-Low($\overline{E}_0$,$\overline{E}_1$) and one active High(E_2). Every output will be High unless $\overline{E}_0$ and $\overline{E}_1$ are Low and E_2 is High. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'ALS138s and one inverter. The device can be used as an eight output demultiplexer by using one of the active-Low Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active-High or active-Low state.

ORDERING INFORMATION

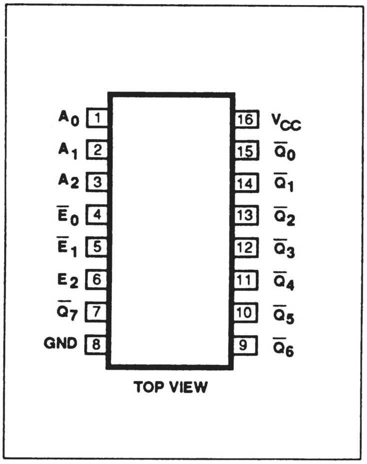
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74ALS138N
16-Pin Plastic SO	N74ALS138D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

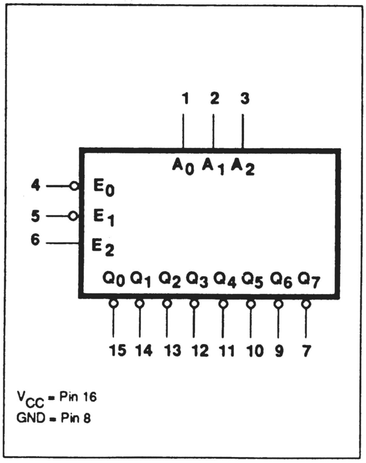
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_2	Address inputs	1.0/1.0	20µA/0.1mA
$\overline{E}_0$, $\overline{E}_1$	Enable inputs (active Low)	1.0/1.0	20µA/0.1mA
E_2	Enable input (active Low)	1.0/1.0	20µA/0.1mA
$\overline{Q}_0$-$\overline{Q}_7$	Data outputs (active Low)	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

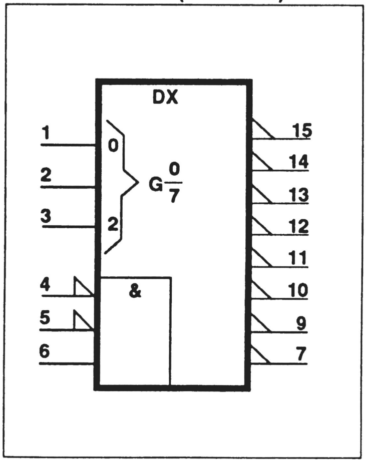


LOGIC SYMBOL

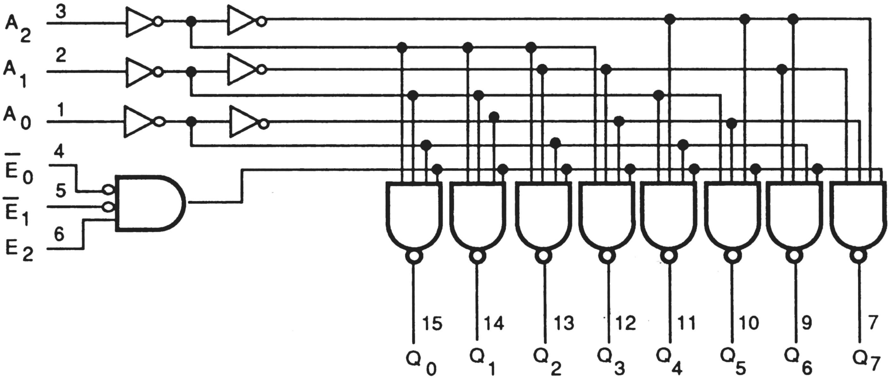


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM


A2
3
A1
2
A0
1
E0
4
5
E1
6
E2
15
Q0
14
Q1
13
Q2
12
Q3
11
Q4
10
Q5
9
Q6
7
Q7

V_{CC} = Pin 16
GND = Pin 8

DECODER FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_0$	$\overline{E}_1$	E_2	A_0	A_1	A_2	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$V_{CC}\pm10\%$, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -0.4mA		V_{CC} - 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.1	mA
$I_O{}^3$	Output current	V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			5	10	mA

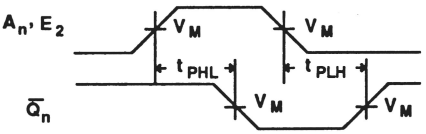
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

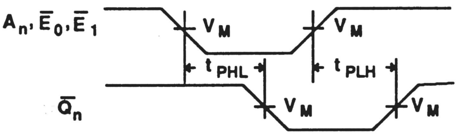
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 1, 2	6 6	22 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to $\overline{Q}_n$	Waveform 2	4 5	17 17	ns
t_{PLH} t_{PHL}	Propagation delay E_2 to $\overline{Q}_n$	Waveform 1	4 5	17 17	ns

AC WAVEFORMS


A_n, E_2
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Q}_n$
V_M
V_M

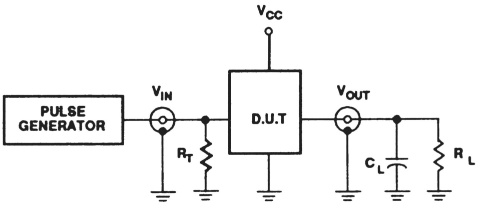
Waveform 1. For Inverting Outputs


A_n, $\overline{E}_0$, $\overline{E}_1$
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Q}_n$
V_M
V_M

Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L

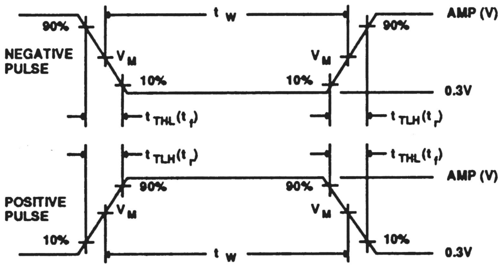
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
V_M
10%
t_w
10%
V_M
90%
AMP (V)
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
AMP (V)
POSITIVE PULSE
90%
V_M
10%
90%
V_M
10%
t_w
0.3V

V_M = 1.3V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS139
Decoder/Demultiplexer

Dual 1-Of-4 Decoder//Demultiplexer

Preliminary Specification

FEATURES

- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Multifunction capability**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS139	9ns	8mA

DESCRIPTION

The 74ALS139 is a dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_{0n}, A_{1n}) and providing four mutually exclusive active-Low outputs ($\overline{Q}_{0n}$ - $\overline{Q}_{3n}$). Each decoder has an active-Low Enable ($\overline{E}$). When $\overline{E}$ is High, every output is forced High. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74ALS139N
16-Pin Plastic SO	N74ALS139D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_{0n}, A_{1n}	Address inputs	1.0/1.0	20µA/0.1mA
$\overline{E}_a$, $\overline{E}_b$	Enable inputs (active Low)	1.0/1.0	20µA/0.1mA
$\overline{Q}_{0n}$-$\overline{Q}_{3n}$	Data outputs (active Low)	20/80	0.4mA/8mA

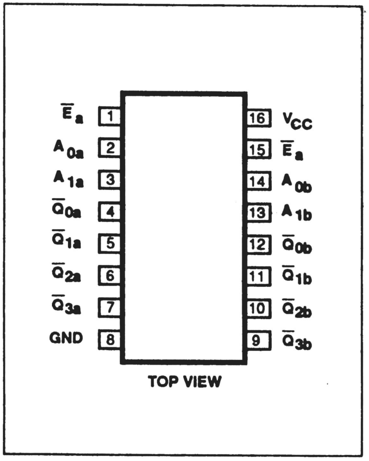
NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

FUNCTION TABLE

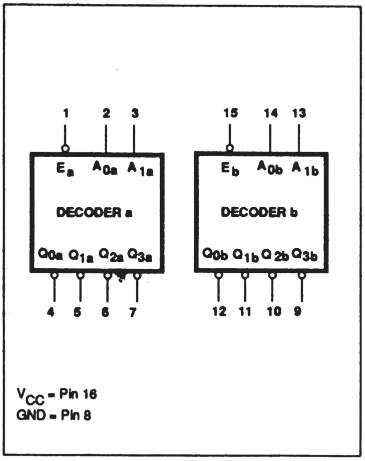
INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

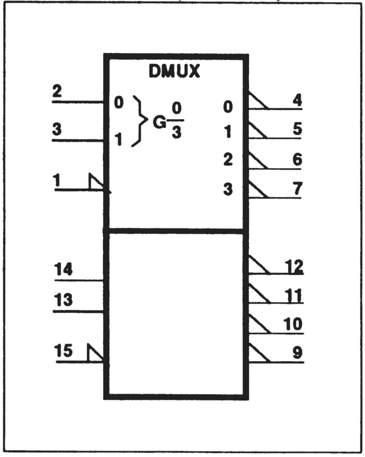
PIN CONFIGURATION


$\overline{E}_a$ 1
A_{0a} 2
A_{1a} 3
$\overline{Q}_{0a}$ 4
$\overline{Q}_{1a}$ 5
$\overline{Q}_{2a}$ 6
$\overline{Q}_{3a}$ 7
GND 8
16 V_{CC}
15 $\overline{E}_a$
14 A_{0b}
13 A_{1b}
12 $\overline{Q}_{0b}$
11 $\overline{Q}_{1b}$
10 $\overline{Q}_{2b}$
9 $\overline{Q}_{3b}$
TOP VIEW

LOGIC SYMBOL

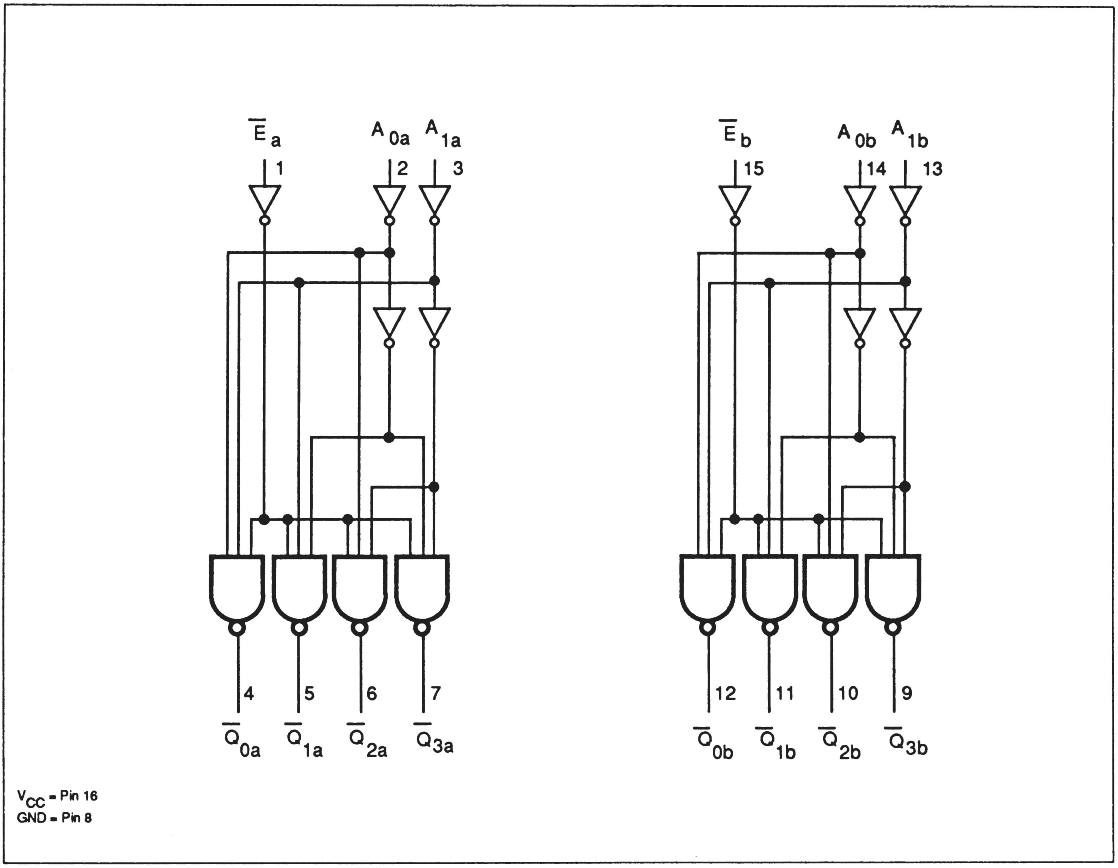

1 2 3
E_a A_{0a} A_{1a}
DECODER a
Q_{0a} Q_{1a} Q_{2a} Q_{3a}
4 5 6 7
15 14 13
E_b A_{0b} A_{1b}
DECODER b
Q_{0b} Q_{1b} Q_{2b} Q_{3b}
12 11 10 9
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)


DMUX
2
3
1
0
1
G $\frac{0}{3}$
0
1
2
3
4
5
6
7
14
13
15
12
11
10
9

August 1988

LOGIC DIAGRAM


$\overline{E}_a$
A_{0a}
A_{1a}
1
2
3
$\overline{E}_b$
A_{0b}
A_{1b}
15
14
13
4
5
6
7
$\overline{Q}_{0a}$
$\overline{Q}_{1a}$
$\overline{Q}_{2a}$
$\overline{Q}_{3a}$
12
11
10
9
$\overline{Q}_{0b}$
$\overline{Q}_{1b}$
$\overline{Q}_{2b}$
$\overline{Q}_{3b}$
V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$V_{CC}\pm10\%$, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -0.4mA		V_{CC} - 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O[3]	Output current	V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			8	13	mA

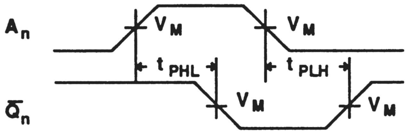
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

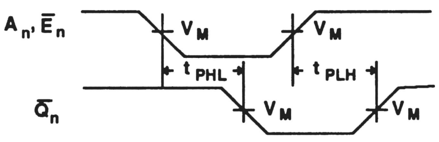
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω Min	 Max	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 1, 2	3 3	14 14	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Q}_n$	Waveform 2	3 3	14 15	ns

AC WAVEFORMS


A_n
V_M
V_M
t_PHL
t_PLH
Q̄_n
V_M
V_M

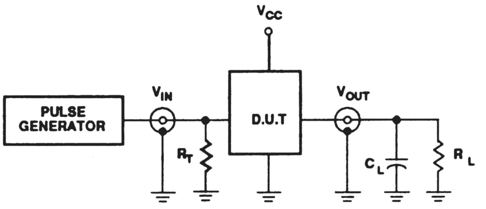
Waveform 1. For Inverting Outputs


A_n, Ē_n
V_M
V_M
t_PHL
t_PLH
Q̄_n
V_M
V_M

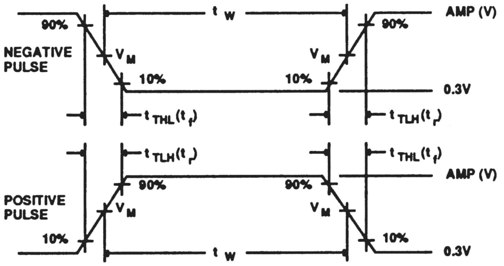
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
R_T
D.U.T
V_OUT
C_L
R_L

Test Circuit For Totem-Pole Outputs


t_W
90%
NEGATIVE PULSE
V_M
10%
V_M
10%
90%
AMP (V)
0.3V
t_THL (t_f)
t_TLH (t_r)
t_TLH (t_r)
t_THL (t_f)
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0.3V
t_W

V_M = 1.3V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	 Rep. Rate	 t_W	 t_{TLH}	 t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS151
Multiplexer

74ALS151 8-Input Multiplexer
Preliminary Specification

FEATURES

- 8-to-1 multiplexing
- On chip decoding
- Multifunction capability
- Complementary outputs
- See 'ALS251 for 3-state version

DESCRIPTION

The 74ALS151 is a logic implementation of a single pole 8-position switch with the switch position controlled by the state of three Select (S_0, S_1,S_2) inputs. True(Y) and complementary ($\overline{Y}$) outputs are both provided. The Enable ($\overline{E}$) is active Low. When $\overline{E}$ is High, the Y output is Low and the $\overline{Y}$ output is High. regardless of all other inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS151	12ns	7.5mA

ORDERING INFORMATION

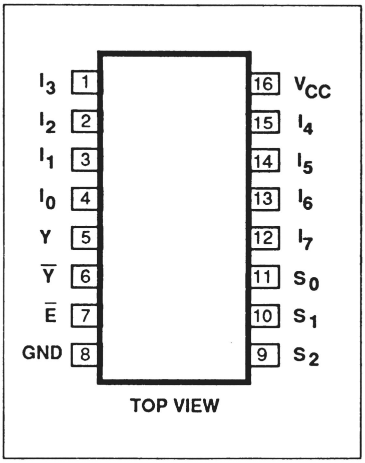
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74ALS151N
16-Pin Plastic SO	N74ALS151D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0- I_7	Data inputs	1.0/1.0	20µA/0.1mA
S_0- S_2	Select inputs	1.0/1.0	20µA/0.1mA
$\overline{E}$	Enable input (active Low)	1.0/1.0	20µA/0.1mA
Y, $\overline{Y}$	Data outputs	130/240	2.6mA/24mA

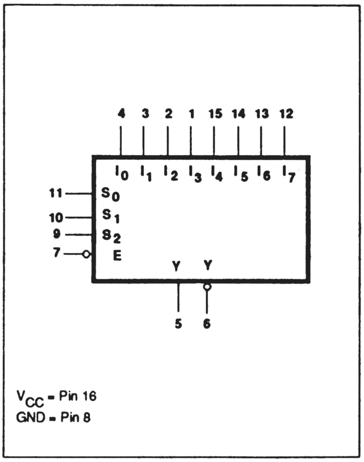
NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION



I_3 1
I_2 2
I_1 3
I_0 4
Y 5
$\overline{Y}$ 6
$\overline{E}$ 7
GND 8
16 V_{CC}
15 I_4
14 I_5
13 I_6
12 I_7
11 S_0
10 S_1
9 S_2
TOP VIEW

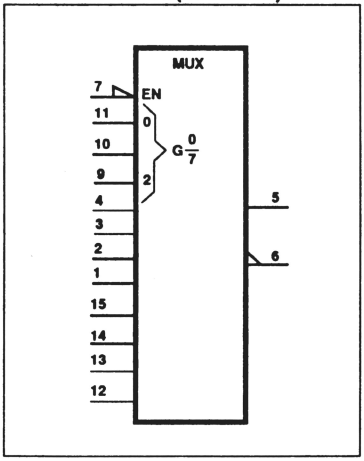
LOGIC SYMBOL



4 3 2 1 15 14 13 12
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7
11 S_0
10 S_1
9 S_2
7 E
Y $\overline{Y}$
5 6

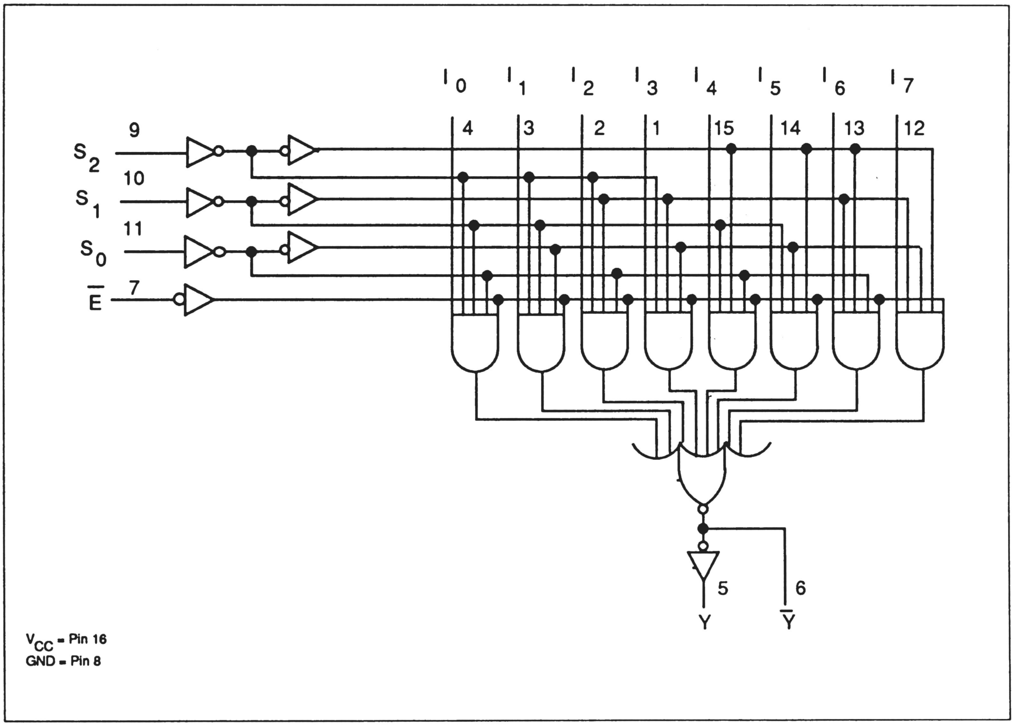
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



MUX
7
EN
11
0
10
G $\frac{0}{7}$
9
2
4
3
2
1
15
14
13
12
5
6

LOGIC DIAGRAM


I0
I1
I2
I3
I4
I5
I6
I7
4
3
2
1
15
14
13
12
S2
9
S1
10
S0
11
E
7
5
6
Y
Y
VCC = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{E}$	Y	$\overline{Y}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC}±10%	V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} - 2			V
		V_{CC} = MIN		I_{OH} = -2.6mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA			0.25	0.4	V
			I_{OL} = 24mA			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$					-1.5	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V					-0.1	mA
I_O[3]	Output current	V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX				7.5	12	mA

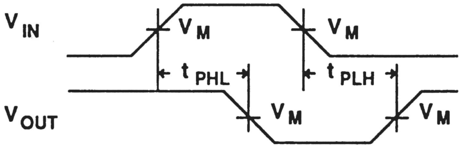
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

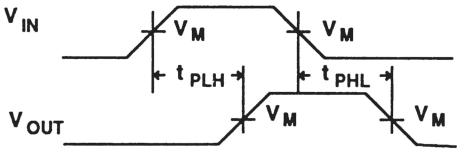
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	Waveform 1	3 5	10 15	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	Waveform 2	3 4	15 15	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	Waveform 1,2	4 8	18 24	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	Waveform 1,2	7 7	23 23	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y	Waveform 1	4 4	18 19	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$	Waveform 1	5 5	19 23	ns

AC WAVEFORMS


V_{IN}
V_M
V_M
t_{PHL}
t_{PLH}
V_{OUT}
V_M
V_M

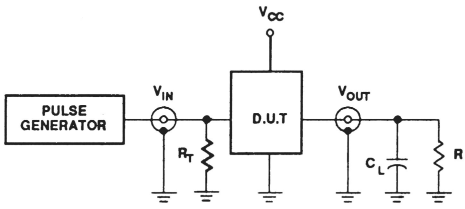
Waveform 1. For Inverting Outputs


V_{IN}
V_M
V_M
t_{PLH}
t_{PHL}
V_{OUT}
V_M
V_M

Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


V_{CC}
V_{IN}
V_{OUT}
PULSE GENERATOR
D.U.T
R_T
C_L
R_L

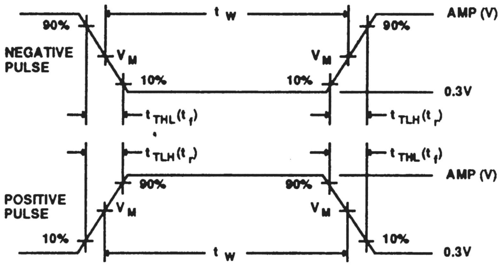
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t_W
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0.3V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0.3V
t_W

V_M = 1.3V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS153
Multiplexer

Dual 4-Input Multiplexer

Preliminary Specification

FEATURES

- **Non-inverting outputs**
- **Common select inputs**
- **Separate enable for each section**
- **See "ALS253 for 3-State version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS153	7ns	7.5mA

DESCRIPTION

The 74ALS153 has two identical 4-input multiplexers with 3-state outputs which select two bits from four sources by using common select inputs (S_0,S_1). The two 4-input multiplexer circuits have individual active-Low Enables ($\overline{E}_a$,$\overline{E}_b$) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced Low when the corresponding enable is High.

The 74ALS153 is the logic implementation of a 2-pole,4-position switch, where the position of the switch is determined by the logic levels supplied to the common select inputs.

ORDERING INFORMATION

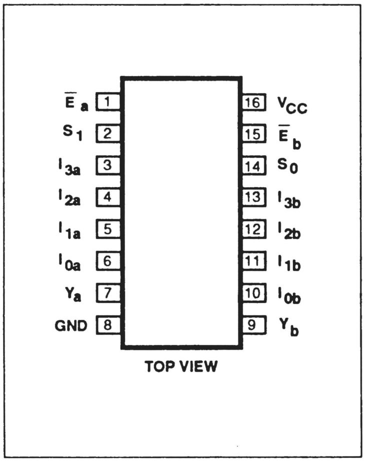
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74ALS153N
16-Pin Plastic SO	N74ALS153D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}- I_{3a}	Port A data inputs	1.0/1.0	20µA/0.1mA
I_{0b}- I_{3b}	Port B data inputs	1.0/1.0	20µA/0.1mA
S_0- S_2	Common Select inputs	1.0/1.0	20µA/0.1mA
$\overline{E}_a$	Port A Enable input (active Low)	1.0/1.0	20µA/0.1mA
$\overline{E}_b$	Port B Enable input (active Low)	1.0/1.0	20µA/0.1mA
Y_a, Y_b	Outputs	130/240	2.6mA/24mA

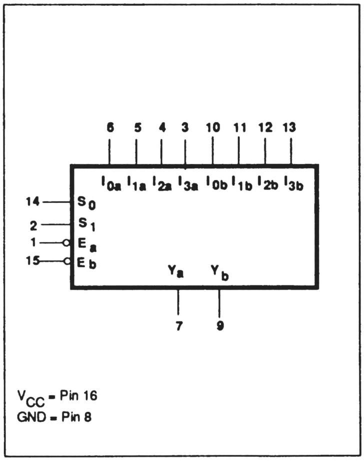
NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION



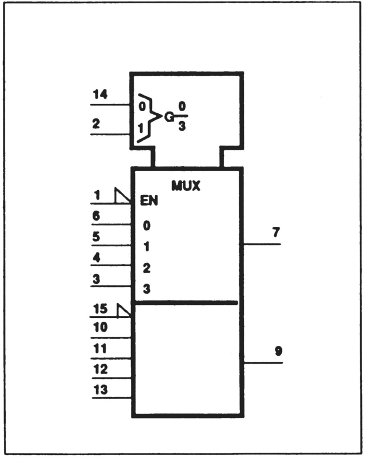
$\overline{E}_a$ 1
S_1 2
I_{3a} 3
I_{2a} 4
I_{1a} 5
I_{0a} 6
Y_a 7
GND 8
16 V_{CC}
15 $\overline{E}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 Y_b
TOP VIEW

LOGIC SYMBOL



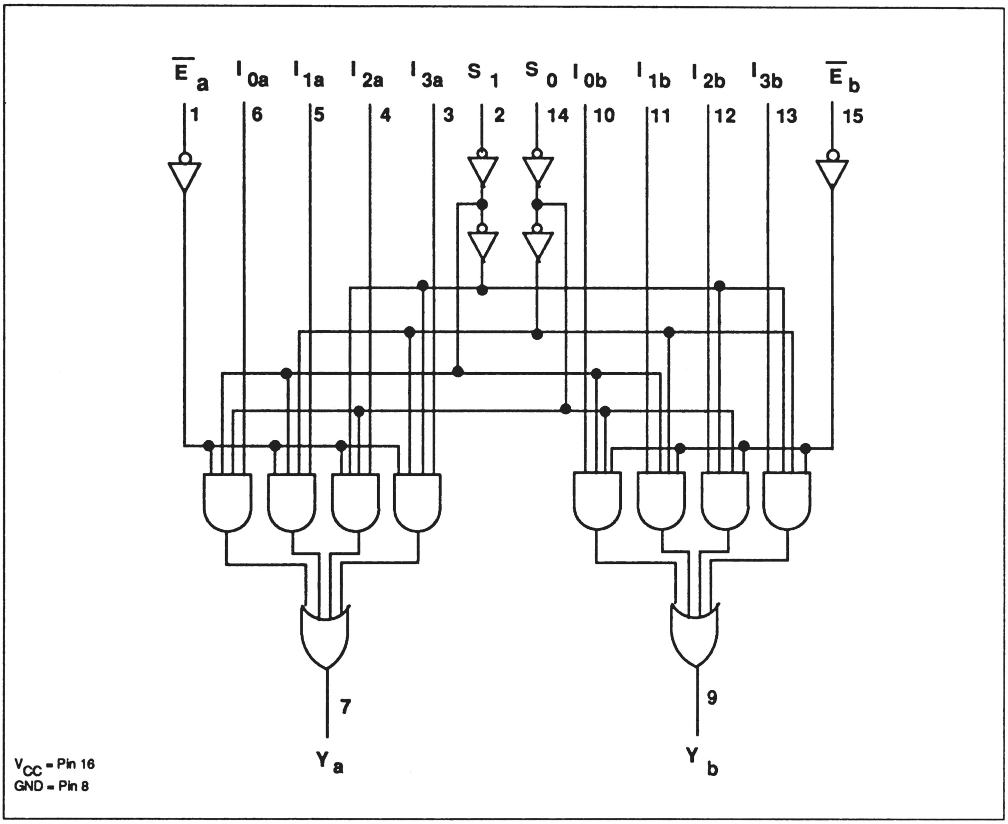
6 5 4 3 10 11 12 13
I_{0a} I_{1a} I_{2a} I_{3a} I_{0b} I_{1b} I_{2b} I_{3b}
14 S_0
2 S_1
1 E_a
15 E_b
Y_a Y_b
7 9
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



14
2
0
1
G $\frac{0}{3}$
MUX
EN
1
6
5
4
3
0
1
2
3
7
15
10
11
12
13
9

LOGIC DIAGRAM


$\overline{E}_a$
I_{0a}
I_{1a}
I_{2a}
I_{3a}
S_1
S_0
I_{0b}
I_{1b}
I_{2b}
I_{3b}
$\overline{E}_b$
1
6
5
4
3
2
14
10
11
12
13
15
7
9
Y_a
Y_b
V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{E}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC}±10%	V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} - 2			V
		V_{CC} = MIN		I_{OH} = -2.6mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA			0.25	0.4	V
			I_{OL} = 24mA			0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.5	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V					-0.1	mA
I_O[3]	Output current	V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX				7.5	14	mA

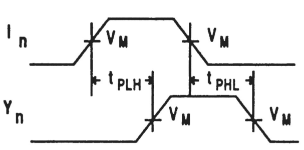
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current,I_{os}.

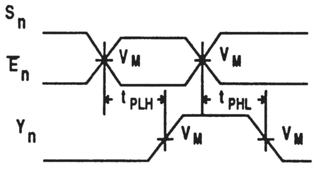
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3 4	10 15	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	Waveform 2	5 5	21 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Y	Waveform 2	5 5	18 18	ns

AC WAVEFORMS


I_n
V_M
V_M
t_{PLH}
t_{PHL}
Y_n
V_M
V_M

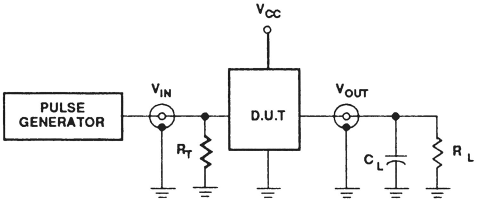
Waveform 1. Propagation Delay
Data to Output


S_n
$\overline{E}_n$
V_M
V_M
t_{PLH}
t_{PHL}
Y_n
V_M
V_M

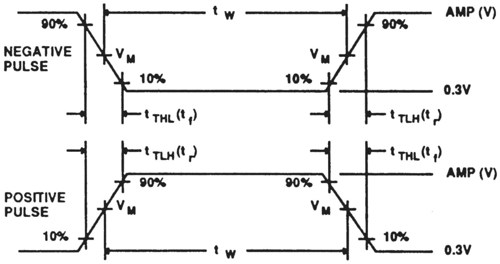
Waveform 2. Propagation Delay
Select or Enable to Output

NOTE: For all waveforms, V_M = 1.3V.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_T
C_L
R_L

Test Circuit For Totem-Pole Outputs


90%
NEGATIVE PULSE
V_M
10%
t_W
V_M
10%
90%
AMP (V)
0.3V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
$t_{TLH}(t_r)$
$t_{THL}(t_f)$
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
t_W
0.3V

V_M = 1.3V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS157, 74ALS158

Data Selectors/Multiplexers

74ALS157 Quad 2-Input DataSelect/Multiplexer, Noninverting
74ALS158 Quad 2-Input Data Selector/Multiplexer, Inverting

Product Specification

DESCRIPTION

The 74ALS157 is a Quad 2-input multiplexer which selects 4 bits of data from one of two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active when Low. When $\overline{E}$ is High, all of the outputs (Y_n) are forced Low regardless of all other input conditions.

Moving data from two registers to a common output bus is a typical use of the 74ALS157. The state of the Select input determines the particular register from which the data comes.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The 74ALS158 is similar but has inverting outputs ($\overline{Y}_n$).

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS157	6.0ns	6mA
74ALS158	6.0ns	6mA

ORDERING INFORMATION

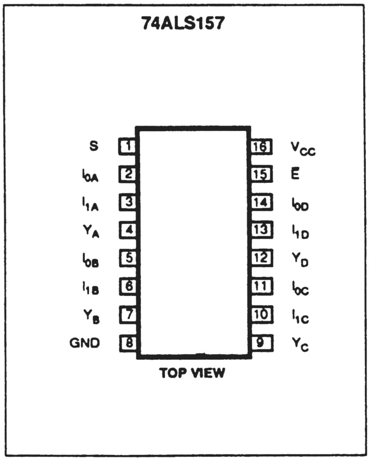
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-pin Plastic DIP	N74ALS157N, N74ALS158N
16-pin Plastic SO	N74ALS157D, N74ALS158D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

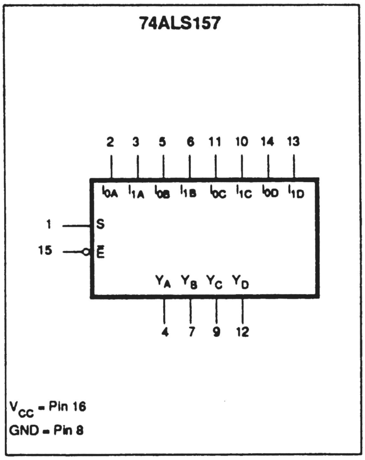
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{nA}, I_{nB}, I_{nC}	Data inputs	1.0/1.0	20µA/0.1mA
S	Select input	1.0/1.0	20µA/0.1mA
$\overline{E}$	Enable input	1.0/1.0	20µA/0.1mA
Y_A - Y_D, $\overline{Y}_A$ - $\overline{Y}_D$	Data outputs	20/240	0.4mA/24mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

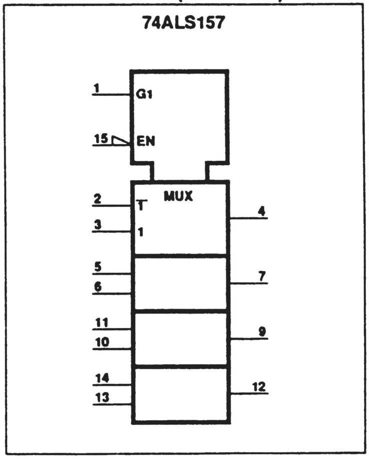
PIN CONFIGURATION


74ALS157
S 1
I0A 2
I1A 3
YA 4
I0B 5
I1B 6
YB 7
GND 8
16 VCC
15 E
14 I0D
13 I1D
12 YD
11 I0C
10 I1C
9 YC
TOP VIEW

LOGIC SYMBOL

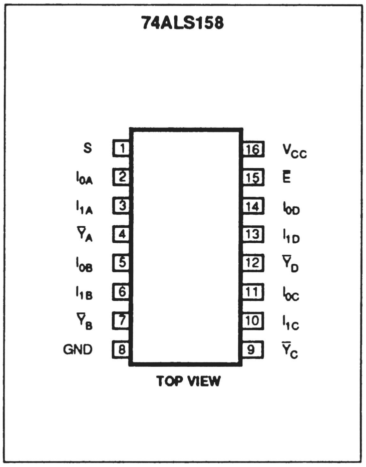

74ALS157
2 3 5 6 11 10 14 13
I0A I1A I0B I1B I0C I1C I0D I1D
1 S
15 E
YA YB YC YD
4 7 9 12
VCC = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)

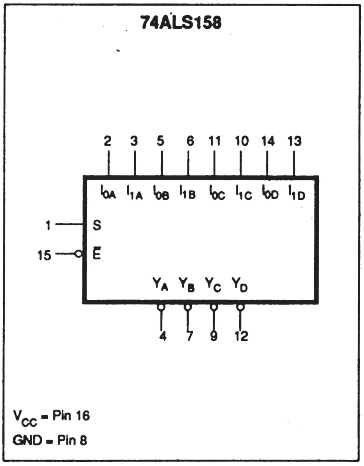

74ALS157
1 G1
15 EN
MUX
2 T
3 1
4
5
6
7
11
10
9
14
13
12

Data Selectors/Multiplexers 74ALS157, 74ALS158

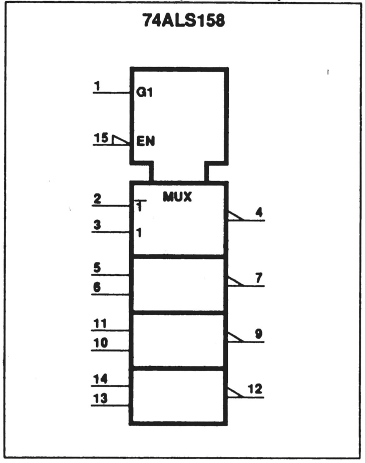
PIN CONFIGURATION


74ALS158
S 1
I_{0A} 2
I_{1A} 3
$\bar{Y}_A$ 4
I_{0B} 5
I_{1B} 6
$\bar{Y}_B$ 7
GND 8
16 V_{CC}
15 $\bar{E}$
14 I_{0D}
13 I_{1D}
12 $\bar{Y}_D$
11 I_{0C}
10 I_{1C}
9 $\bar{Y}_C$
TOP VIEW

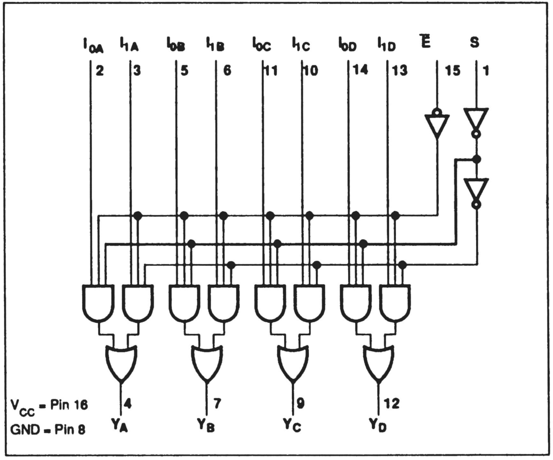
LOGIC SYMBOL


74ALS158
2 3 5 6 11 10 14 13
I_{0A} I_{1A} I_{0B} I_{1B} I_{0C} I_{1C} I_{0D} I_{1D}
1 S
15 $\bar{E}$
Y_A Y_B Y_C Y_D
4 7 9 12
V_{CC} = Pin 16
GND = Pin 8

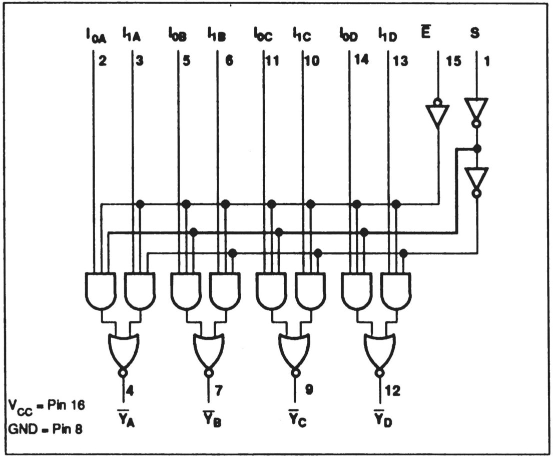
LOGIC SYMBOL(IEEE/IEC)


74ALS158
1 G1
15 EN
MUX
2 $\bar{1}$
3 1
4
5
6
7
11
10
9
14
13
12

LOGIC DIAGRAM, 74ALS157


I_{0A} 2
I_{1A} 3
I_{0B} 5
I_{1B} 6
I_{0C} 11
I_{1C} 10
I_{0D} 14
I_{1D} 13
$\bar{E}$ 15
S 1
V_{CC} = Pin 16
GND = Pin 8
4 Y_A
7 Y_B
9 Y_C
12 Y_D

LOGIC DIAGRAM, 74ALS158


I_{0A} 2
I_{1A} 3
I_{0B} 5
I_{1B} 6
I_{0C} 11
I_{1C} 10
I_{0D} 14
I_{1D} 13
$\bar{E}$ 15
S 1
V_{CC} = Pin 16
GND = Pin 8
4 $\bar{Y}_A$
7 $\bar{Y}_B$
9 $\bar{Y}_C$
12 $\bar{Y}_D$

FUNCTION TABLE

INPUTS				OUTPUT
$\bar{E}$	S	I_{0n}	I_{1n}	Y_n
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE

INPUTS				OUTPUT
$\bar{E}$	S	I_{0n}	I_{1n}	$\bar{Y}_n$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	V_{CC}-2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O[3]	Output current		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	74ALS157	V_{CC} = MAX			6	11	mA
		74ALS158				6	10	mA

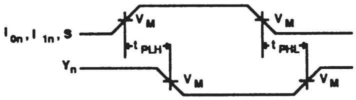
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current,I_{OS}.

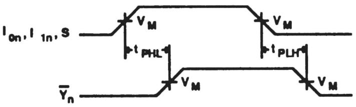
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay I_{0n} or I_{1n} to Y_n	74ALS157	Waveform 1	2.0 2.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Y_n		Waveform 1, 3	4.0 4.0	12 12	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y_n		Waveform 3	4.0 7.0	11 14	ns
t_{PLH} t_{PHL}	Propagation delay I_{0n} or I_{1n} to $\overline{Y}_n$	74ALS158	Waveform 2	2.0 2.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$		Waveform 2, 4	4.0 4.0	12 12	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}_n$		Waveform 4	4.0 4.0	14 14	ns

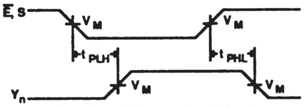
AC WAVEFORMS


I0n, I1n, S
Yn
VM
VM
tPLH
tPHL
VM
VM

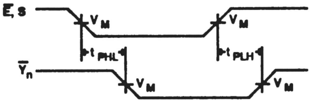
Waveform 1. Propagation Delay For Data And Select To Output


I0n, I1n, S
Ȳn
VM
VM
tPHL
tPLH
VM
VM

Waveform 2. Propagation Delay For Data And Select To Output


Ē, S
Yn
VM
VM
tPLH
tPHL
VM
VM

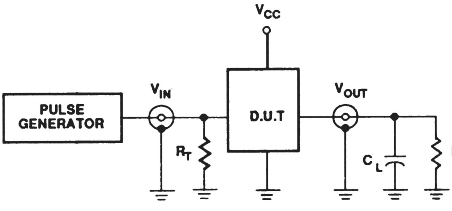
Waveform 3. Propagation Delay For Enable And Select To Output


Ē, S
Ȳn
VM
VM
tPHL
tPLH
VM
VM

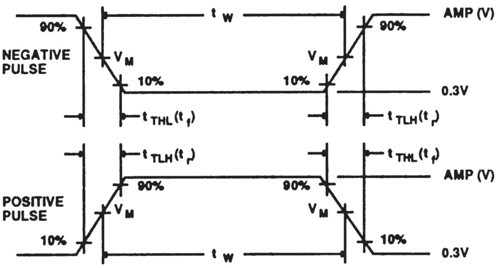
Waveform 4. Propagation Delay For Enable And Select To Output

NOTE: For all waveforms, V_M = 1.3V.

TEST CIRCUIT AND WAVEFORMS


VCC
VIN
VOUT
PULSE GENERATOR
D.U.T
RT
CL
RL

Test Circuit For Totem-Pole Outputs


tW
AMP (V)
90%
90%
NEGATIVE PULSE
VM
VM
10%
10%
0.3V
tTHL(tf)
tTLH(tr)
tTLH(tr)
tTHL(tf)
AMP (V)
90%
90%
POSITIVE PULSE
VM
VM
10%
10%
0.3V
tW

V_M = 1.3V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS161B,74ALS163B Counters

4-Bit Binary Counters

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS161B	140MHz	10mA
74ALS163B	140MHz	10mA

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous Reset ('ALS161B)**
- **Synchronous Reset ('ALS163B)**
- **High speed synchronous expansion**
- **Typical count rate of 140MHz**

DESCRIPTION

Synchronous presettable 4-bit binary counters ('ALS161B, 'ALS163B) feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The clock input is buffered.

The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0-D_3 inputs to be loaded into the counter on the positive-going edge of the clock (provided that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all the four outputs of the flip-flops (Q_0-Q_3) in 'ALS161B to Low levels, regardless of the levels at CP,$\overline{PE}$,CET and CEP inputs (thus providing an asynchronous clear function). For the 'ALS163B the clear function is synchronous. A Low level at the Synchronous Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q_0-Q_3) to Low levels after the next positive-going transition on the clock (CP) input (provided that the setup and hold time requirements for $\overline{SR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. The synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A). The carry look-ahead simplifies serial cascading of the counters. Both Count Enable (CEP and CET) inputs must be High to

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	74ALS161BN, 74ALS163BN
16-Pin Plastic SO	74ALS161BD, 74ALS163BD

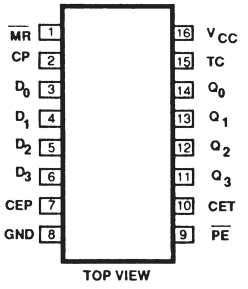
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20μA/0.1mA
CEP	Count Enable Parallel input	1.0/1.0	20 A/0.1mA
CET	Count Enable Trickle input	1.0/1.0	20 A/0.1mA
CP	Clock input (active rising edge)	1.0/1.0	20 A/0.1mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20μA/0.1mA
$\overline{MR}$	Asynchronous Master Reset input (active Low) for 'ALS161B	1.0/1.0	20μA/0.1mA
$\overline{SR}$	Synchronous Reset input (active Low) for 'ALS163B	1.0/1.0	20μA/0.1mA
TC	Terminal count output	20/80	0.4mA/8mA
Q_0 -Q_3	Flip-flop outputs	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20μA in the High state and 0.1mA in the Low state.

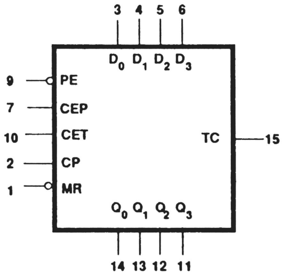
PIN CONFIGURATION

'ALS161B



LOGIC SYMBOL

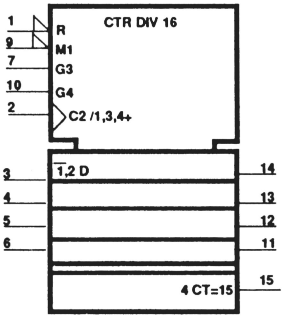
'ALS161B



V_{CC} = Pin 16
GND = Pin 8

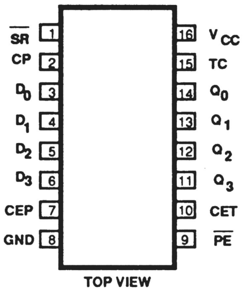
LOGIC SYMBOL(IEEE/IEC)

'ALS161B



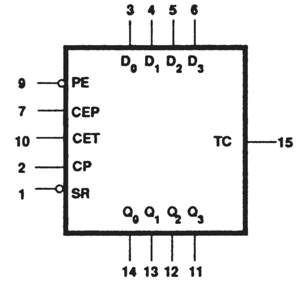
PIN CONFIGURATION

'ALS163B


SR 1
CP 2
D0 3
D1 4
D2 5
D3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE
TOP VIEW

LOGIC SYMBOL

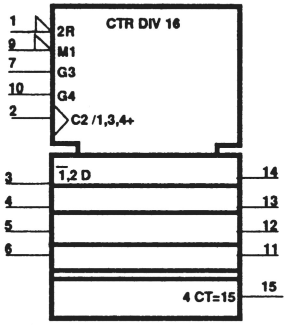
'ALS163B


3 4 5 6
D0 D1 D2 D3
9 PE
7 CEP
10 CET
2 CP
1 SR
TC 15
Q0 Q1 Q2 Q3
14 13 12 11

V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)

'ALS163B


CTR DIV 16
1 2R
9 M1
7 G3
10 G4
2 C2 /1,3,4+
3 1,2 D 14
4 13
5 12
6 11
4 CT=15 15

count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure B). The TC output is subjected to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

APPLICATIONS

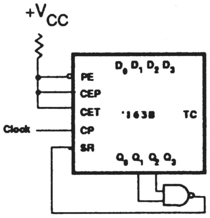

+VCC
D0 D1 D2 D3
PE
CEP
CET
'163B
TC
Clock
CP
SR
Q0 Q1 Q2 Q3

Fig. A maximum count modifying scheme
Terminal count = 6

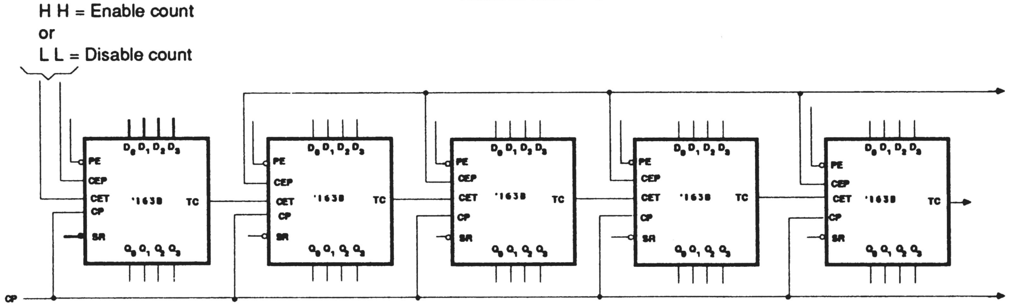

H H = Enable count
or
L L = Disable count
D0 D1 D2 D3
PE
CEP
CET
CP
SR
'163B
TC
Q0 Q1 Q2 Q3
CP

Fig. B Synchronous multistage counting scheme

MODE SELECT-FUNCTION TABLE for 'ALS161B

INPUTS						OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC	
L	X	X	X	X	X	L	L	Reset (clear)
H	↑	X	X	l	l	L	L	Parallel load
H	↑	X	X	l	h	H	(a)	
H	↑	h	h	h	X	count	(a)	Count
H	X	l	X	h	X	q_n	(a)	Hold (do nothing)
H	X	X	l	h	X	q_n	L	

MODE SELECT-FUNCTION TABLE for 'ALS163B

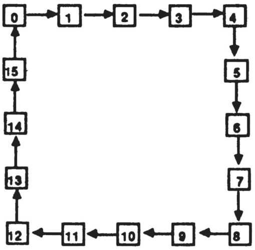
INPUTS						OUTPUTS		OPERATING MODE
$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC	
l	↑	X	X	X	X	L	L	Reset (clear)
h	↑	X	X	l	l	L	L	Parallel load
h	↑	X	X	l	h	H	(a)	
h	↑	h	h	h	X	count	(a)	Count
h	X	l	X	h	X	q_n	(a)	Hold (do nothing)
h	X	X	l	h	X	q_n	L	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(a) = The TC output is High when CET is High and the counter is at Terminal Count (HHHH)

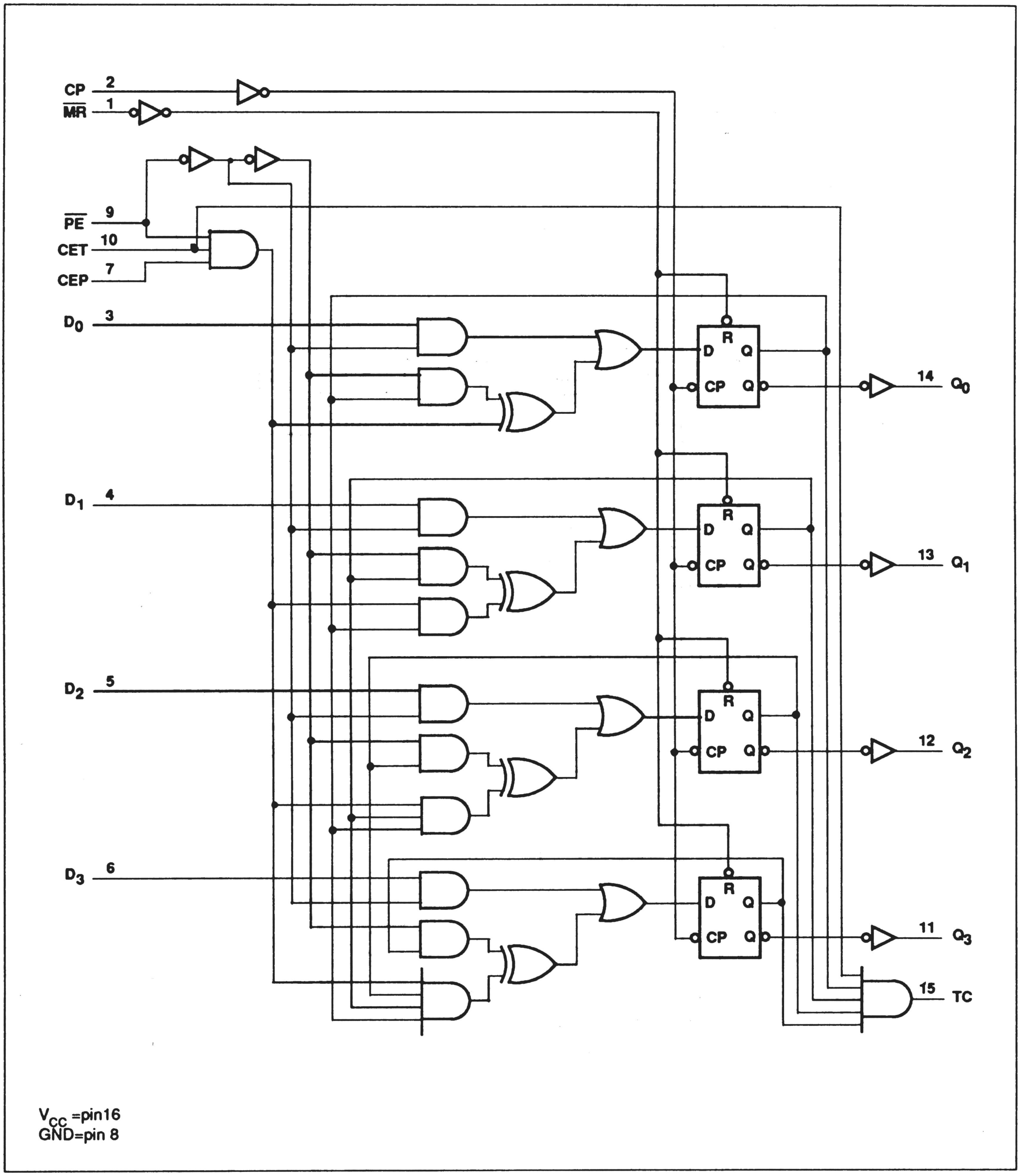
STATE DIAGRAM

Logic equations: Count Enable=$CEP \cdot CET \cdot \overline{PE}$

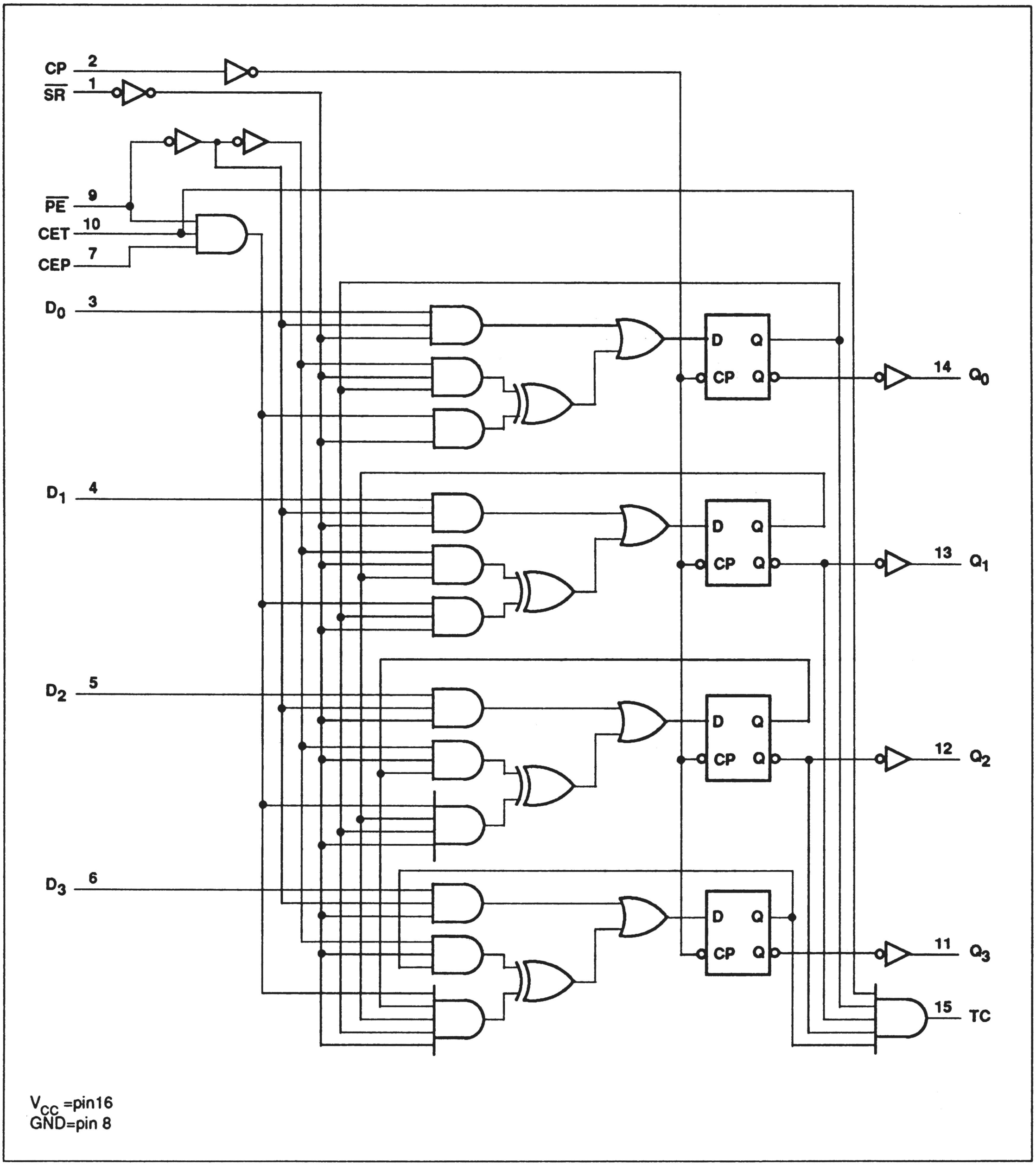
$TC=Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$



LOGIC DIAGRAM for 'ALS161B


CP 2
MR 1
PE 9
CET 10
CEP 7
D0 3
D1 4
D2 5
D3 6
R
D
Q
CP
14 Q0
13 Q1
12 Q2
11 Q3
15 TC
VCC =pin16
GND=pin 8

LOGIC DIAGRAM for 'ALS163B


CP 2
SR 1
PE 9
CET 10
CEP 7
D0 3
D1 4
D2 5
D3 6
D Q
CP Q
14 Q0
13 Q1
12 Q2
11 Q3
15 TC
VCC =pin16
GND=pin 8

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$V_{CC}\pm10\%$, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -0.4mA		V_{CC} - 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O[3]	Output current	V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			10	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

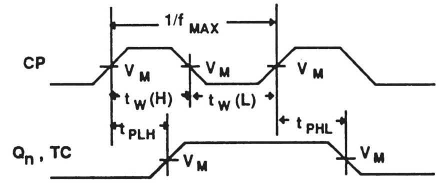
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
				Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4 6	13 16	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	6 8	16 16	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	3 3	10 10	ns
t_{PHL}	Propagation delay $\overline{\text{MR}}$ to Q_n	'161B	Waveform 3	8	15	ns
t_{PHL}	Propagation delay $\overline{\text{MR}}$ to TC	'161B	Waveform 3	11	19	ns

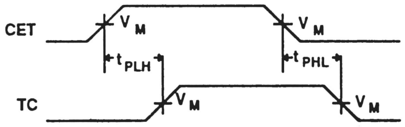
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 6	8 8		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	Waveform 6	0 0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{\text{PE}}$ or $\overline{\text{SR}}$ to CP	Waveform 5 or 6	10 10		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{\text{PE}}$ or $\overline{\text{SR}}$ to CP	Waveform 5 or 6	0 0		ns
t_s(H) t_s(L)	Setup time, High or Low CET or CEP to CP	Waveform 4	10 10		ns
t_h(H) t_h(L)	Hold time, High or Low CET or CEP to CP	Waveform 4	0 0		ns
t_w(H) t_w(L)	CP pulse width (Load) High or Low	Waveform 1	5 5		ns
t_w(H) t_w(L)	CP pulse width (Count) High or Low	Waveform 1	5 5		ns
t_wL)	$\overline{\text{MR}}$ or $\overline{\text{SR}}$ pulse width, Low	Waveform 3	5		ns
t_{REC}	Recovery time, $\overline{\text{MR}}$ or $\overline{\text{SR}}$ to CP	Waveform 3	10		ns

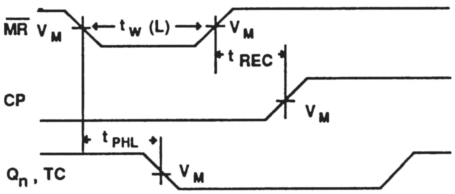
AC WAVEFORMS


1/f MAX
CP
V M
t w (H)
t w (L)
t PLH
t PHL
Qn , TC

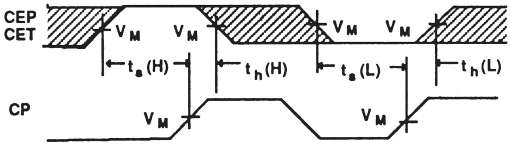
Waveform 1.
Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency


CET
V M
t PLH
t PHL
TC

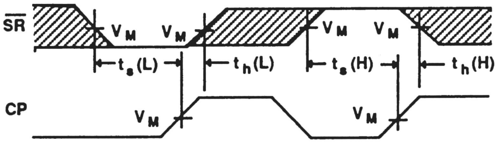
Waveform 2.
Propagation Delay, CET Input to TC Output


MR
V M
t w (L)
t REC
CP
t PHL
Qn , TC

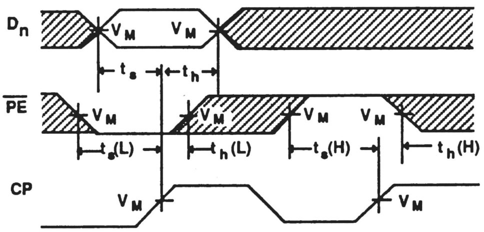
Waveform 3.
Master Reset pulse width, Master Reset to Output Delay and Master Reset to Recovery Time


CEP
CET
V M
t s (H)
t h (H)
t s (L)
t h (L)
CP

Waveform 4.
CEP and CET Reset Setup and Hold Times


SR
V M
t s (L)
t h (L)
t s (H)
t h (H)
CP

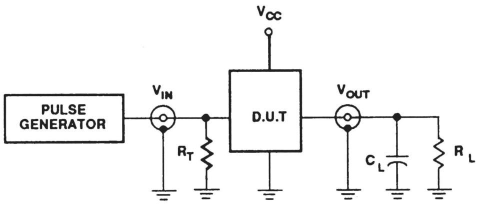
Waveform 5.
Synchronous Reset Setup and Hold Times


Dn
V M
t s
t h
PE
t s (L)
t h (L)
t s (H)
t h (H)
CP

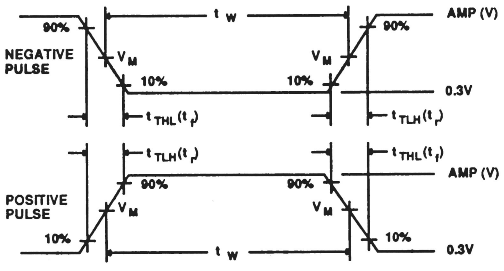
Waveform 6.
Parallel Data and Parallel Enable Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.3V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L

Test Circuit For Totem-Pole Outputs


t w
AMP (V)
90%
NEGATIVE PULSE
V M
10%
0.3V
t THL (t f)
t TLH (t r)
POSITIVE PULSE

$V_M = 1.3V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS164
Shift Register

8-Bit Serial-In Parallel-Out Shift Register
Preliminary Specification

FEATURES

- **Gated serial data inputs**
- **Typical shift frequency of 60 MHz**
- **Asynchronous Master Reset**
- **Buffered Clock and Data Inputs**
- **Fully synchronous data transfer**

DESCRIPTION

The 74ALS164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa}, D_{sb}); either input can be used as an active-High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs (D_{sa}, D_{sb}) that existed one setup time before the rising clock edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS164	60 MHz	3.5 mA

ORDERING INFORMATION

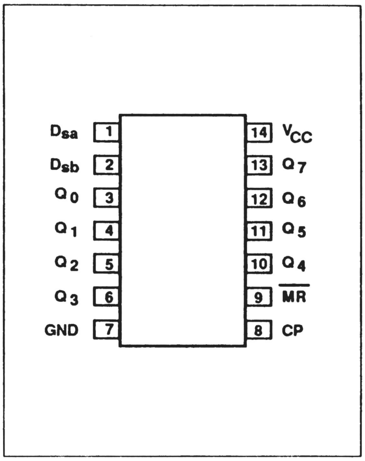
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	74ALS164N
14-Pin Plastic SO	74ALS164D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

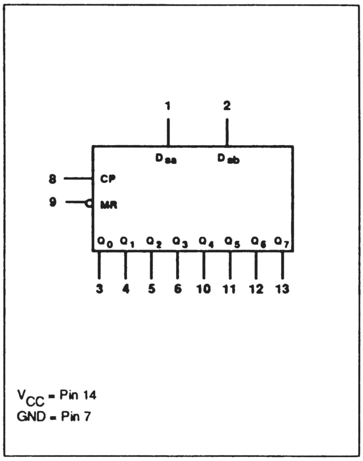
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{sa}, D_{sb}	Data inputs	1.0/1.0	20µA/0.1mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.1mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20µA/0.1mA
Q_0-Q_7	Outputs	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

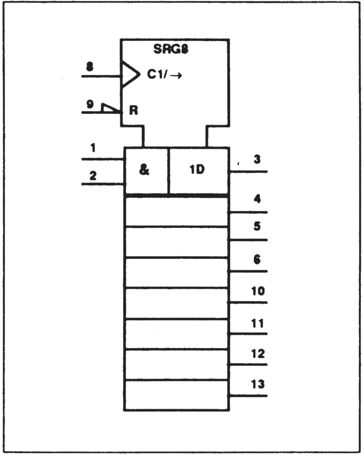


LOGIC SYMBOL



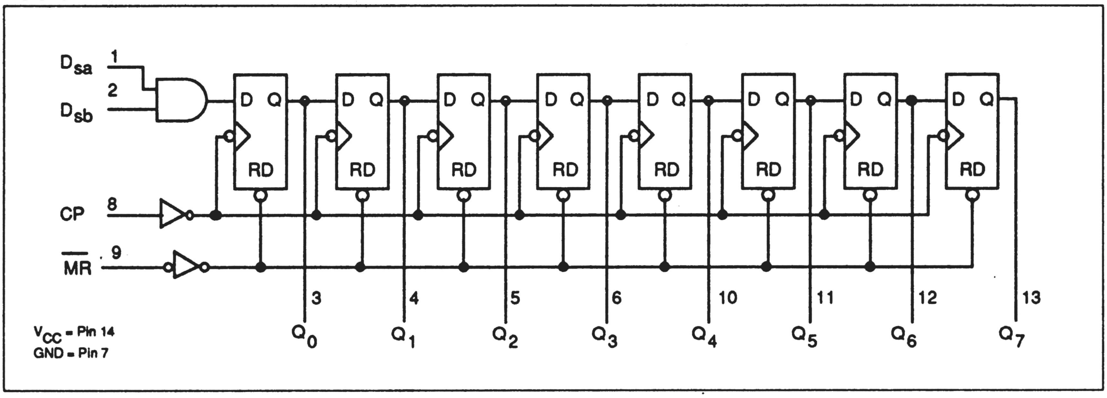
V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL(IEEE/IEC)



August 16, 1988

LOGIC DIAGRAM

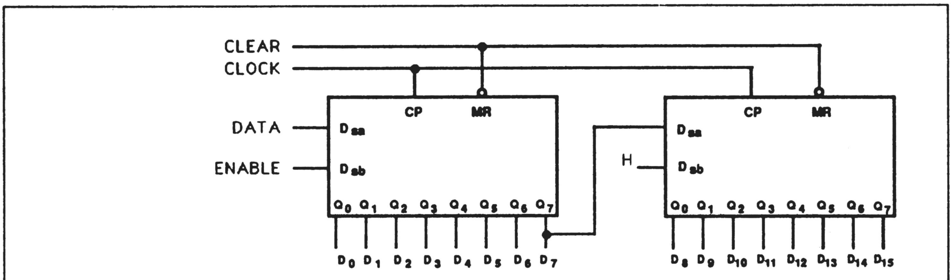

D_{sa} 1
2 D_{sb}
CP 8
$\overline{MR}$ 9
D Q
RD
3 Q_0
4 Q_1
5 Q_2
6 Q_3
10 Q_4
11 Q_5
12 Q_6
13 Q_7
V_{CC} = Pin 14
GND = Pin 7

FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1 ---- Q_7	
L	X	X	X	L	L L	Reset (clear)
H	↑	l	l	L	q_0 q_6	Shift
H	↑	l	h	L	q_0 q_6	
H	↑	h	l	L	q_0 q_6	
H	↑	h	h	H	q_0 q_6	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

APPLICATION


CLEAR
CLOCK
DATA
ENABLE
H
CP
MR
D_{sa}
D_{sb}
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
D_8 D_9 D_{10} D_{11} D_{12} D_{13} D_{14} D_{15}

NOTES:
The 'ALS164 can be cascaded to form synchronous shift registers of any length. Here, two devices are combined to form a 16-bit shift register.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$V_{CC}\pm10\%$, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}-2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	I_{OL} = 4mA		0.25	0.4	V
		V_{IH} = MIN	I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O[3]	Output current	V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			10		mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

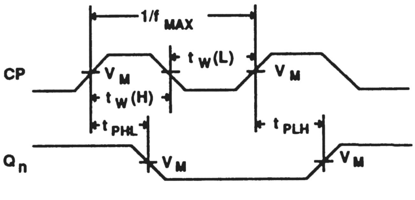
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	45		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 4.0	12.0 12.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	2.0	10.0	ns

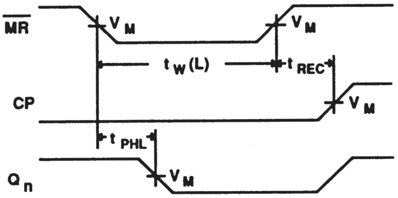
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	Waveform 3 Waveform 3	10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP	Waveform 3 Waveform 3	0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1 Waveform 1	10.0 10.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	10.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	6.0		ns

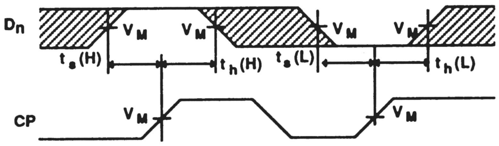
AC WAVEFORM



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



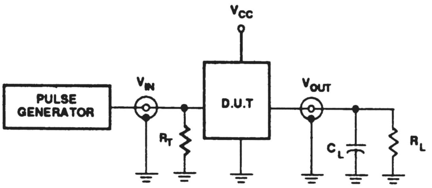
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



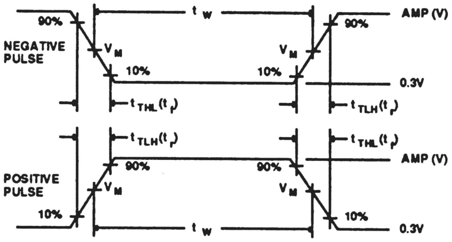
Waveform 3. Data Setup And Hold Times

NOTE: For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
D.U.T
V_OUT
R_T
C_L
R_L

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
90%
V_M
10%
t_w
AMP (V)
0.3V
t_THL (t_f)
t_TLH (t_r)
POSITIVE PULSE
90%
V_M
10%
t_w
AMP (V)
0.3V
t_TLH (t_r)
t_THL (t_f)

$V_M = 1.3V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS174
Flip-Flop

Hex D Flip-Flops

Preliminary Specification

FEATURES

- **Six edge-triggered D-type flip-flops**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**

DESCRIPTION

The 74ALS174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where true outputs only are required, and the Clock and Master Reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS174	60 MHz	11 mA

ORDERING INFORMATION

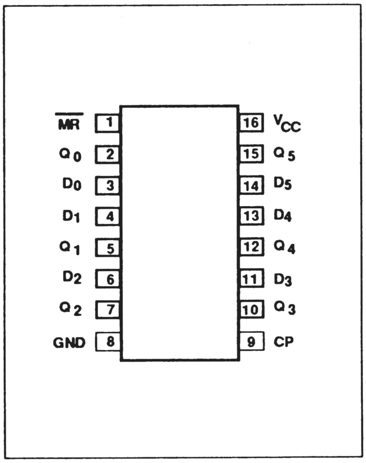
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	74ALS174N
16-Pin Plastic SO	74ALS174D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_5	Data inputs	1.0/1.0	20μA/0.1mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20 A/0.1mA
$\overline{MR}$	Master Reset input(active-Low)	1.0/1.0	20μA/0.1mA
Q_0-Q_5	Outputs	20/80	0.4mA/8mA

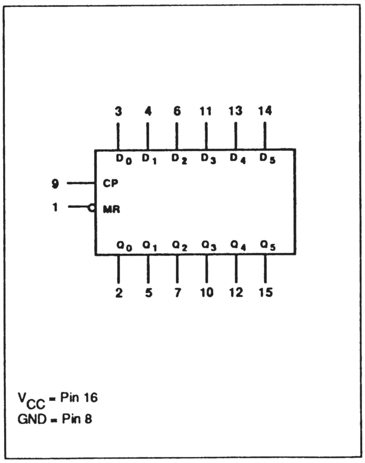
NOTE:
One (1.0) ALS Unit Load is defined as: 20μA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION



$\overline{MR}$ 1
Q0 2
D0 3
D1 4
Q1 5
D2 6
Q2 7
GND 8
16 VCC
15 Q5
14 D5
13 D4
12 Q4
11 D3
10 Q3
9 CP

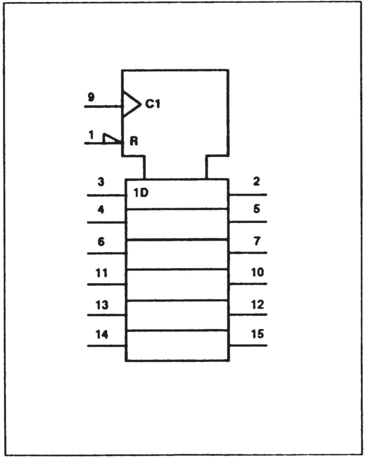
LOGIC SYMBOL



3 4 6 11 13 14
D0 D1 D2 D3 D4 D5
9 CP
1 MR
Q0 Q1 Q2 Q3 Q4 Q5
2 5 7 10 12 15

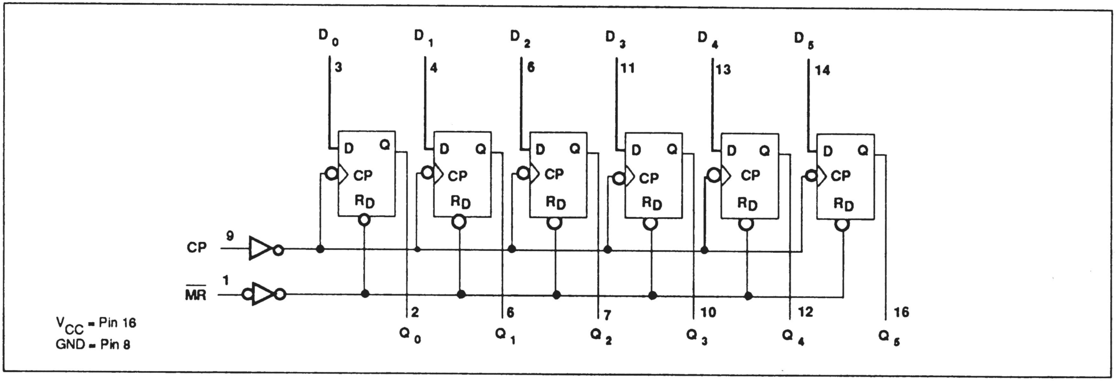
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



9
C1
1
R
3
1D
2
4
5
6
7
11
10
13
12
14
15

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	D	Q_n	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
L = Low voltage level
X = Don't care
↑= Low-to-High Clock transition
h =High voltage level one set-up time prior to the Low-to-High Clock transition.
l = Low voltage level one set-up time prior to the Low-to-High Clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level outputvoltage	V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}-2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O[3]	Output current	V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			11	19	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{os}.

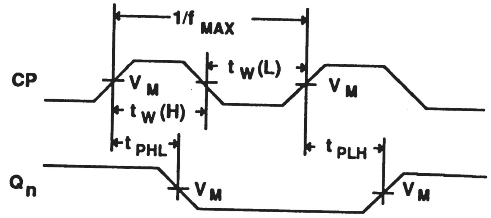
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 5.0	15.0 17.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	8.0	23.0	ns

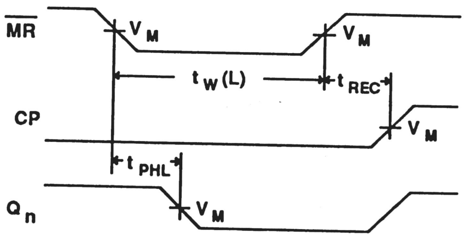
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	Waveform 3 Waveform 3	10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP	Waveform 3 Waveform 3	0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1 Waveform 1	10.0 10.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	10.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	6.0		ns

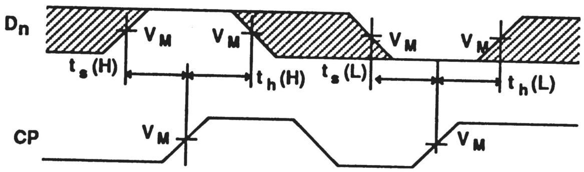
AC WAVEFORM


1/f MAX
CP
V M
t w(L)
V M
t w(H)
t PHL
t PLH
Q n
V M
V M

Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


MR
V M
V M
t w(L)
t REC
CP
V M
t PHL
Q n
V M

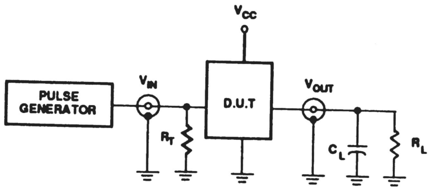
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


D n
V M
V M
V M
V M
t s (H)
t h (H)
t s (L)
t h (L)
CP
V M
V M

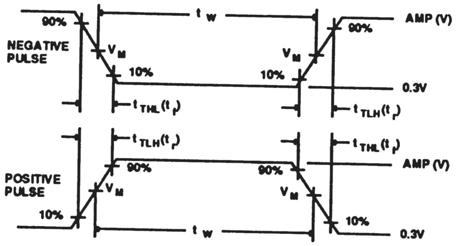
Waveform 3. Data Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.3V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L

Test Circuit for Totem-Pole Outputs


90%
NEGATIVE PULSE
V M
10%
t w
AMP (V)
90%
V M
10%
0.3V
t THL (t f)
t TLH (t r)
t TLH (t r)
t THL (t f)
90%
90%
AMP (V)
POSITIVE PULSE
V M
V M
10%
10%
t w
0.3V

$V_M = 1.3V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS175

Flip-Flop

Quad D Flip-Flops
Preliminary Specification

FEATURES

- **Four edge-triggered D flip- flops**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**
- **True and complementary outputs**

DESCRIPTION

The 74ALS175 is a quad, edge-triggered D-type flip-flops with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both trueand complement outputs are required, and the Clock and Master Reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS175	60 MHz	11 mA

ORDERING INFORMATION

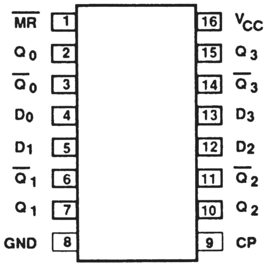
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	74ALS175N
16-Pin Plastic SO	74ALS175D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

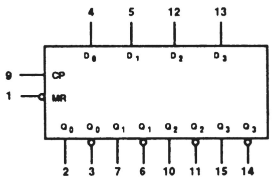
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.1mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20 A/0.1mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20µA/0.1mA
Q_0-Q_3	True outputs	20/80	0.4mA/8mA
$\overline{Q}_0$-$\overline{Q}_3$	Complementary outputs	20/80	0.4mA/8mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

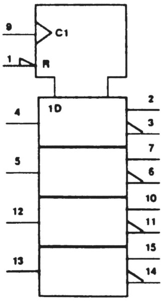

$\overline{MR}$ 1
Q_0 2
$\overline{Q}_0$ 3
D_0 4
D_1 5
$\overline{Q}_1$ 6
Q_1 7
GND 8
16 V_{CC}
15 Q_3
14 $\overline{Q}_3$
13 D_3
12 D_2
11 $\overline{Q}_2$
10 Q_2
9 CP

LOGIC SYMBOL


4
5
12
13
D_0
D_1
D_2
D_3
9
CP
1
MR
Q_0
Q_0
Q_1
Q_1
Q_2
Q_2
Q_3
Q_3
2
3
7
6
10
11
15
14

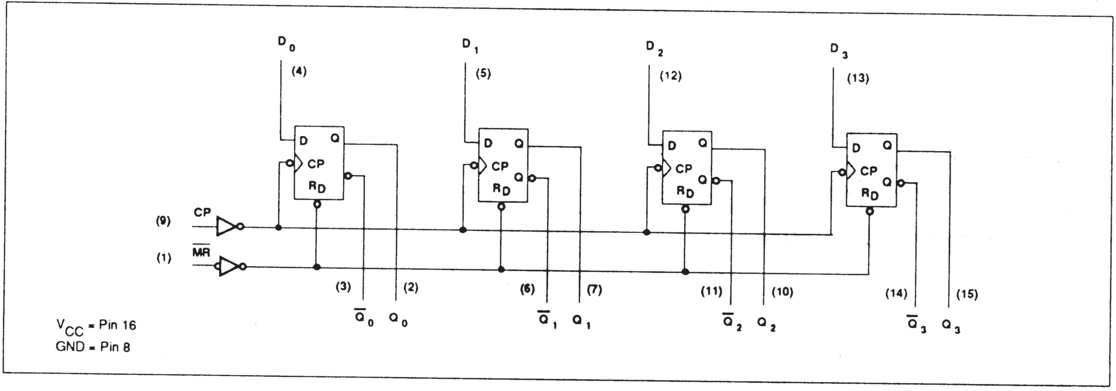
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)


9
C1
1
R
1D
4
5
12
13
2
3
7
6
10
11
15
14

February 1988

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = High voltage level
L = Low voltage level
X = Don't care
↑= Low-to-High Clock transition
h =High voltage level one set-up time prior to the Low-to-High Clock transition.
l = Low voltage level one set-up time prior to the Low-to-High Clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		V_{CC}-2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	I_{OL} = 4mA		0.25	0.4	V
		V_{IH} = MIN	I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O[3]	Output current	V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			9	14	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

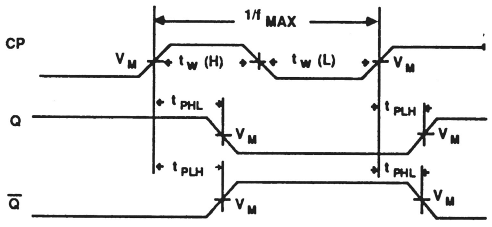
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	3.0 5.0	15.0 17.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	5.0	18.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 2	8.0	23.0	ns

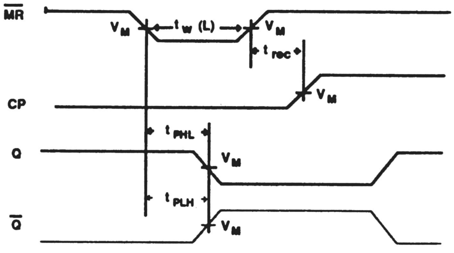
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
t_s(H) t_s(L)	Set-up time D_n to CP	Waveform 3 Waveform 3	10.0 10.0		ns
t_h(H) t_h(L)	Hold time D_n to CP	Waveform 3 Waveform 3	0 0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low	Waveform 1 Waveform 1	10.0 10.0		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 2	10.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	6.0		ns

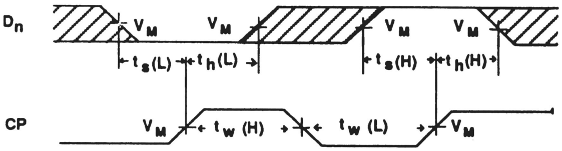
AC WAVEFORM


CP
Q
Q̄
1/f MAX
V_M
t_W (H)
t_W (L)
t_PHL
t_PLH

Waveform 1. Clock to output delay and clock pulse width


MR̄
CP
Q
Q̄
V_M
t_W (L)
t_rec
t_PHL
t_PLH

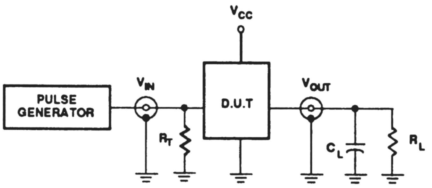
Waveform 2. Master reset to output delay, reset pulse width, and master reset to clock recovery time


D_n
CP
V_M
t_s(L)
t_h(L)
t_s(H)
t_h(H)
t_W (H)
t_W (L)

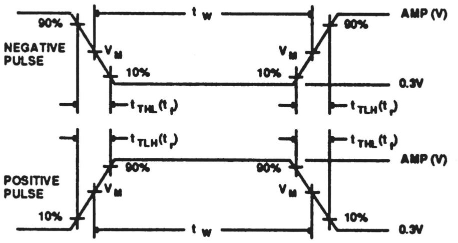
Waveform 3. Data setup time and hold times

NOTE: For all waveforms, $V_M = 1.3V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
R_T
D.U.T
V_OUT
C_L
R_L

Test Circuit for Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_W
t_THL (t_f)
t_TLH (t_r)
AMP (V)
0.3V

$V_M = 1.3V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS191
Counter

Up/Down Binary Counter With Reset and Ripple Clock

Preliminary Specification

FEATURES

- **Synchronous, reversible counting**
- **Asynchronous parallel load capability**
- **Cascadable without external logic**
- **Single up/down control input**

DESCRIPTION

The 74ALS191 is a presettable 4-bit Binary up/down Counter. It contains four edge-triggered master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count up and count down operations. Asynchronous parallel load capability permits the counter to preset to any desired number. Information present on the parallel data inputs (D_0-D_3) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is Low. This operation overrides the counting function. Counting is inhibited by a High level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is Low, internal state changes are initiated. Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$).

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS191	40MHz	12mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	74ALS191N
16-Pin Plastic SO	74ALS191D

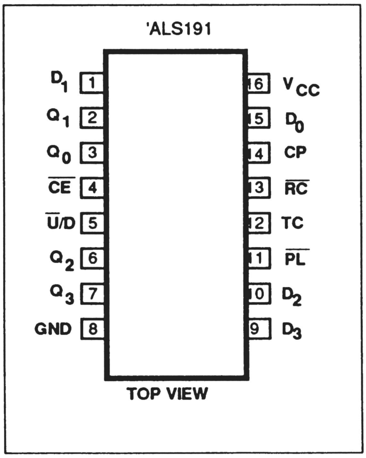
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20μA/0.1mA
$\overline{CE}$	Count enable input (active Low)	1.0/1.0	20μA/0.1mA
CP	Clock input (active rising edge)	1.0/1.0	20μA/0.1mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20μA/0.1mA
$\overline{U}$/D	Up/Down count control input	1.0/1.0	20μA/0.1mA
Q_0 -Q_3	Flip-flop outputs	20/80	0.4mA/8mA
$\overline{RC}$	Ripple clock output (active Low)	20/80	0.4mA/8mA
TC	Terminal count output	20/80	0.4mA/8mA

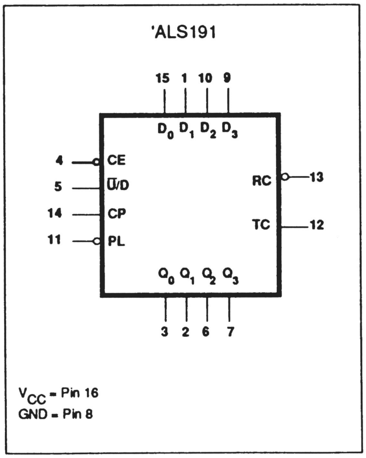
NOTE:
One (1.0) ALS Unit Load is defined as: 20μA in the High state and 0.1mA in the Low state.

The TC output is normally Low and goes High when the count reaches zero in the countdown mode or "15" in the count up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output,. When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the clock pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays.

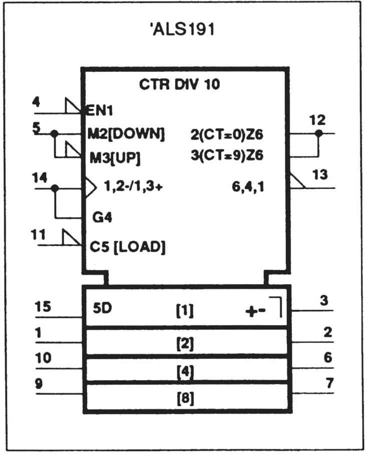
PIN CONFIGURATION



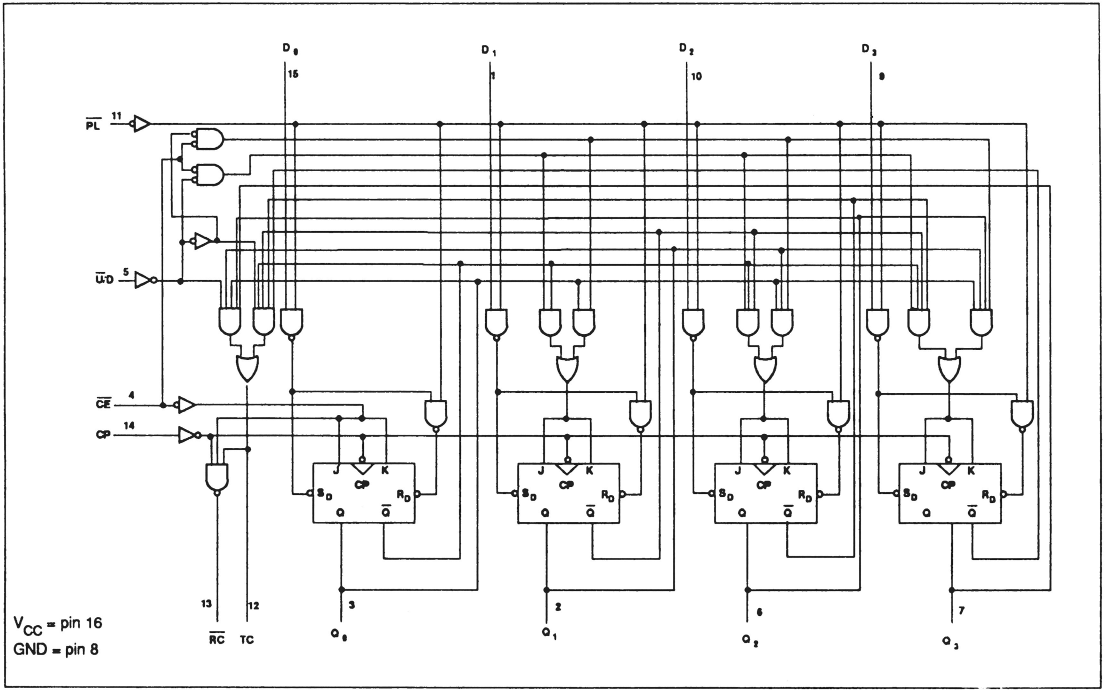
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM


D0
15
D1
1
D2
10
D3
9
PL 11
U/D 5
CE 4
CP 14
J
K
CP
S_D
R_D
Q
$\overline{Q}$
13
12
RC
TC
3
Q0
2
Q1
6
Q2
7
Q3
V_{CC} = pin 16
GND = pin 8

MODE SELECTION FUNCTION TABLE

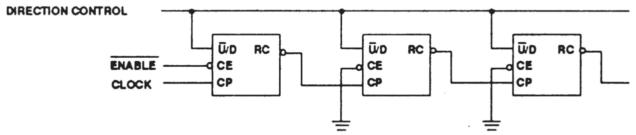
INPUTS					OUTPUT	OPERATING MODE
$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n	
L	X	X	X	L	L	Parallel load
L	X	X	X	H	H	
H	L	l	↑	X	Count up	Count up
H	H	l	↑	X	Count down	Count down
H	X	H	X	X	No change	Hold (do nothing)

TC and $\overline{RC}$ FUNCTION TABLE

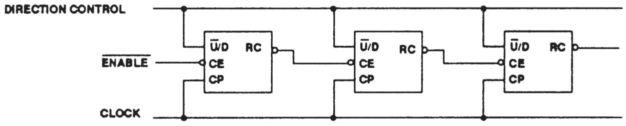
INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	↓	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	↓	⊔

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
⊔ = Low pulse
↓ = High-to-Low clock transition

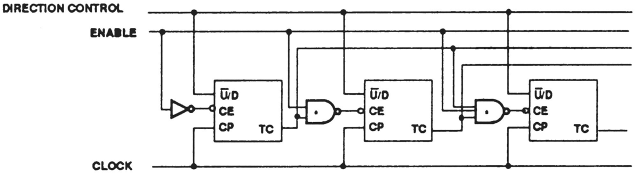
APPLICATIONS



a. N-stage using Ripple Clock



b. Synchronous N-stage Counter with Common Clock using Ripple /Clock



c. Synchronous N-stage Counter with Common Clock and Parrallel Gated Terminal Count

* = Carry Gate

Figure 1

The 'ALS191 simplifies the design of multi-stage counters, as indicated in Figures 1a and 1b. In Figure 1a, each $\overline{RC}$ output is used as the clock input for the next higher stage. When the clock input source has limited drive capability this configuration is particulary advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first stage and the last stages is represented by the cumulative delay of the clock as it ripples-through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ output signals propagate in ripple fashion and all clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative going edge of the $\overline{RC}$ signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its clock input goes High, there is no restriction on the High state duration of the clock.

In the Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. The combined TC signals from all the preceding stages forms the $\overline{CE}$ input signal for given stage. An enable signal signal must also be included in each carry gate in order to inhibit counting. Since the TC output of a given stage is not affected by its own $\overline{CE}$, the simple scheme of Figure 1a and 1b does not apply.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -0.4mA		V_{CC} - 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			-0.73	-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O[3]	Output current	V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			12	22	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

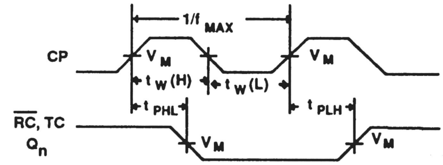
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3 3	18 18	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	8 8	31 31	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{\text{RC}}$	Waveform 2	5 5	20 20	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CE}}$ to $\overline{\text{RC}}$	Waveform 2	4 4	18 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{U}}$/D to $\overline{\text{RC}}$	Waveform 2	15 10	37 28	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{U}}$/D to TC	Waveform 4	8 8	25 25	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Any Output	Waveform 3	4 4	21 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{PL}}$ to Any Output	Waveform 5	8 8	30 30	ns

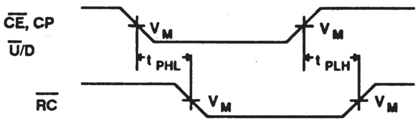
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{\text{PL}}$	Waveform 6	20 20		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{\text{PL}}$	Waveform 6	5 5		ns
$t_s(L)$	Setup time, Low $\overline{\text{CE}}$ to CP	Waveform 6	20		ns
$t_h(L)$	Hold time, Low $\overline{\text{CE}}$ to CP	Waveform 6	0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{\text{U}}$/D to CP	Waveform 6	20 20		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{\text{U}}$/D to CP	Waveform 6	0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	16.5 16.5		ns
$t_w(L)$	$\overline{\text{PL}}$ Pulse width, Low	Waveform 5	20		ns
t_{REC}	Recovery time $\overline{\text{PL}}$ to CP	Waveform 5	20		ns

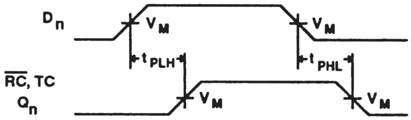
AC WAVEFORMS


1/f MAX
CP
V M
t W (H)
t W (L)
t PHL
t PLH
RC, TC
Q n
V M

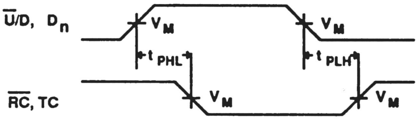
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


CE, CP
U/D
V M
t PHL
t PLH
RC
V M

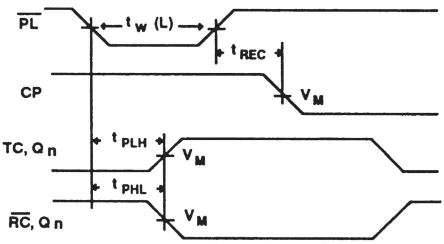
Waveform 2. Propagation Delay, Clock, Clock Enable or Up/Down to Ripple Clock Output


D n
V M
t PLH
t PHL
RC, TC
Q n
V M

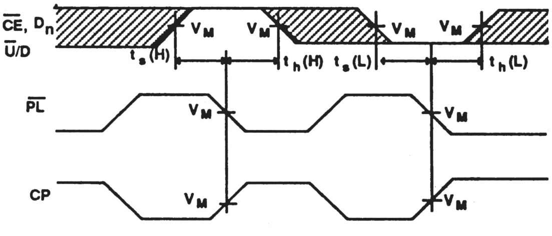
Waveform 3. Propagation Delay, Non-Inverting Path


U/D, D n
V M
t PHL
t PLH
RC, TC
V M

Waveform 4. Propagation Delay, Inverting Path


PL
t w (L)
t REC
CP
V M
TC, Q n
t PLH
t PHL
RC, Q n
V M

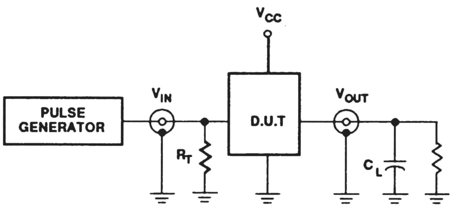
Waveform 5. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time


CE, D n
U/D
V M
t s (H)
t h (H)
t s (L)
t h (L)
PL
CP
V M

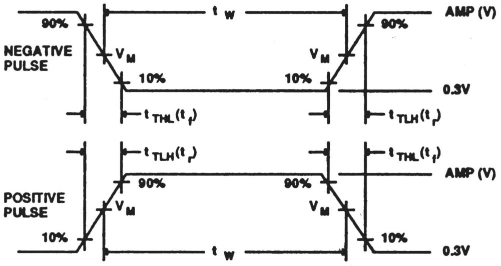
Waveform 6. Data Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.3V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L

Test Circuit For Totem-Pole Outputs


NEGATIVE PULSE
90%
t w
AMP (V)
V M
10%
0.3V
t THL (t f)
t TLH (t r)
POSITIVE PULSE
90%
10%
V M
AMP (V)
0.3V
t w

$V_M = 1.3V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS193
Counter

Synchronous Presettable 4-Bit Binary Counter With Seperate Up and Down Clocks

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS193	40MHz	12mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74ALS193N
16-Pin Plastic SO	N74ALS193D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.1mA
CP_U	Count up clock (active rising edge)	1.0/1.0	20µA/0.1mA
CP_D	Count down clock (active rising edge)	1.0/1.0	20µA/0.1mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20µA/0.1mA
MR	Asynchronous master reset input	1.0/1.0	20µA/0.1mA
Q_0 -Q_3	Flip-flop outputs	20/80	0.4mA/8mA
$\overline{TC}_U$	Terminal count up output (active Low)	20/80	0.4mA/8mA
$\overline{TC}_D$	Terminal count down output (active Low)	20/80	0.4mA/8mA

NOTE:

One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

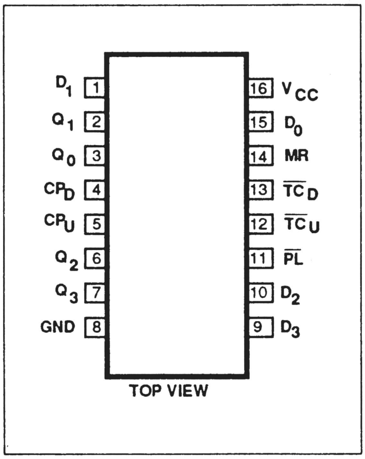
FEATURES

- **Synchronous, reversible counting**
- **Asynchronous parallel load capability**
- **Cascadable without external logic**
- **Asynchronous reset (clear)**

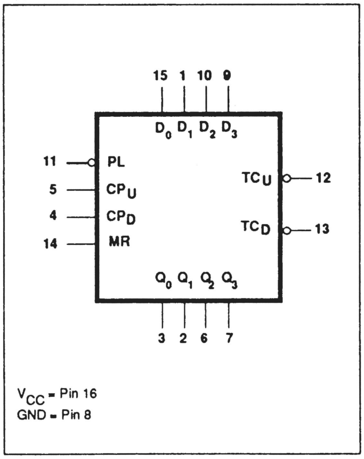
DESCRIPTION

The 74ALS193 is a presettable 4-bit Binary up/down Counter. Seperate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the Low-to-High transition of either Clock input. If the CP_U clock is pulsed while CP_D is held High, the device will count up...if CP_D is pulsed while CP_U is held High, the device will count down. The device can be cleared at any time by the asynchronous reset pin -- it may also be loaded in parallel by activating the asynchronous parallel load pin. Inside the device are four master/slave JK flip-flops with the necessary steering logic to provide asynchronous reset, preset load, and synchronous count up and count down functions. One clock must be held High while counting with the other to avoid either counting by two's or not at all, depending on the state of the first JK flip-flop which cannot toggle as long as either clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts. The Terminal Count outputs ($\overline{TC}_U$ and $\overline{TC}_D$) are normally High. When the circuit has reached the maximum count of 15, the next High-to-Low transistion of CP_U will cause $\overline{TC}_U$ to go Low. $\overline{TC}_U$ will stay Low until CP_U goes High again. Likewise, the $\overline{TC}_D$ output will go Low when the circuit is in the zero state and the CP_D goes Low. The $\overline{TC}$ outputs can be used as a clock signal to the next higher order circuit in a multistage counter, but will be delayed by two-gate delays from the original CP signal. When the asynchronous Parallel Load ($\overline{PL}$) or Master Reset (MR) is active it will override the clock inputs, unless the clock is already Low. In that case, the next Low-to-High transition of that clock will be interpreted as a legitimate signal and will be counted.

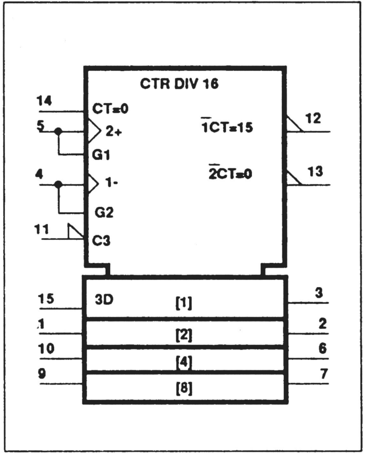
PIN CONFIGURATION



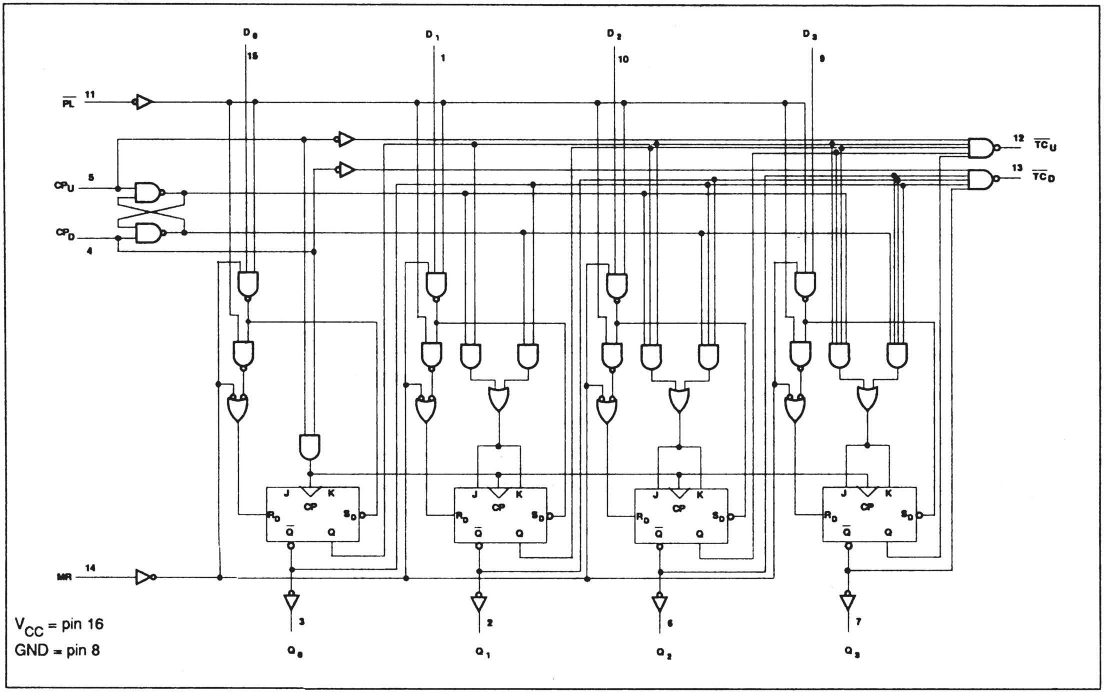
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 16
GND = pin 8

MODE SELECTION TABLE

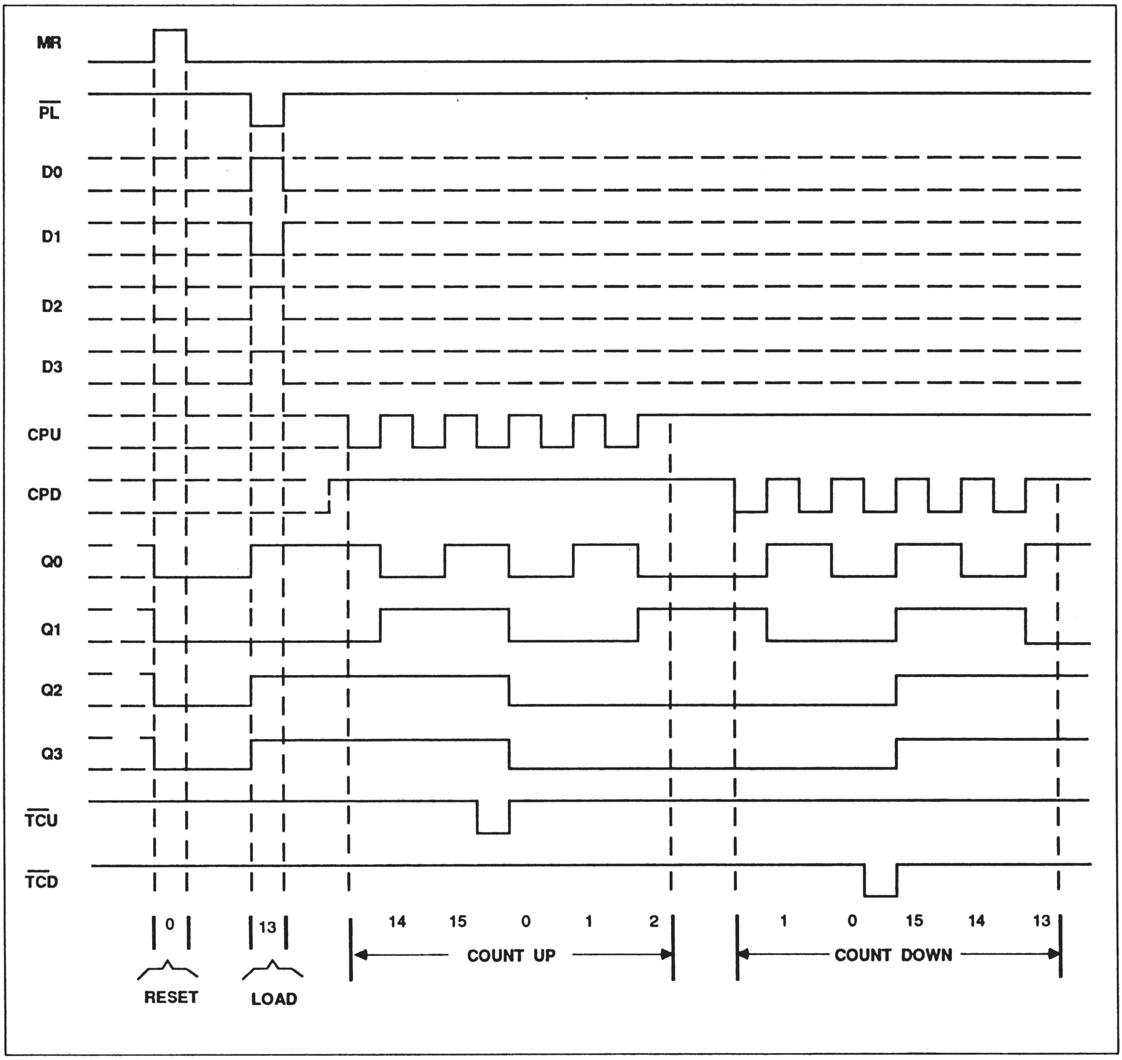
INPUTS								OUTPUTS						OPERATING MODE
MR	$\overline{PL}$	CP_U	CP_D	D0	D1	D2	D3	Q0	Q1	Q2	Q3	$\overline{TC}_U$	$\overline{TC}_D$	
H	X	X	L	X	X	X	X	L	L	L	L	H	L	Reset (clear)
H	X	X	H	X	X	X	X	L	L	L	L	H	H	
L	L	H	L	L	L	L	L	L	L	L	L	H	L	Parallel load
L	L	X	H	L	L	L	L	L	L	L	L	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	L	H	
L	L	H	X	H	H	H	H	H	H	H	H	H	H	
L	H	↑	H	X	X	X	X	Count up				H[1]	H	Count up
L	H	H	↑	X	X	X	X	Count down				H	H[2]	Count down

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

NOTES:

1. $\overline{TC}_U$ =CP_U at terminal count up (HHHH).
2. $\overline{TC}_D$ =CP_D at terminal count down (LLLL).

FUNCTIONAL WAVEFORMS (Typical reset, load, and count sequences)


MR
PL
D0
D1
D2
D3
CPU
CPD
Q0
Q1
Q2
Q3
TCU
TCD
0
13
14
15
0
1
2
1
0
15
14
13
COUNT UP
COUNT DOWN
RESET
LOAD

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -0.4mA		V_{CC} - 2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_O[3]	Output current	V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			12	22	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

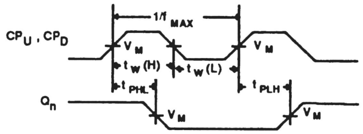
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n	Waveform 1	4 4	19 17	ns
t_{PLH} t_{PHL}	Propagation delay CP_U to $\overline{TC}_U$ or CP_D to $\overline{TC}_D$	Waveform 2	4 5	16 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n	Waveform 4	8 8	30 28	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 4	8 8	30 28	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 3	8 8	30 28	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 3	8 8	30 28	ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 4	5 5	17 17	ns
t_{PLH} t_{PHL}	Propagation delay MR to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 4	8 8	30 28	ns

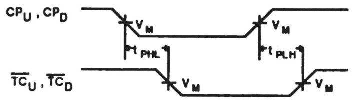
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	20 20		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	5 5		ns
$t_w(H)$ $t_w(L)$	CP_U or CP_D Pulse width, High or Low	Waveform 1	16.5 16.5		ns
$t_w(L)$	CP_U or CP_D Pulse width Low (change of direction)	Waveform 1	20		ns
$t_w(L)$	$\overline{PL}$ Pulse width, Low	Waveform 5	20		ns
$t_w(H)$	MR Pulse width, High	Waveform 4	10		ns
t_{REC}	Recovery time $\overline{PL}$ to CP_U or CP_D	Waveform 5	20		ns
t_{REC}	Recovery time MR to CP_U or CP_D	Waveform 4	20		ns

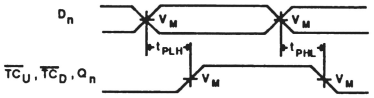
AC WAVEFORMS


CP_U , CP_D
Q_n
1/f MAX
V_M
t_w (H)
t_w (L)
t_PHL
t_PLH

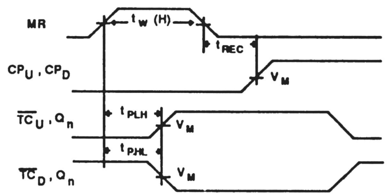
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


CP_U , CP_D
TC_U , TC_D
V_M
t_PHL
t_PLH

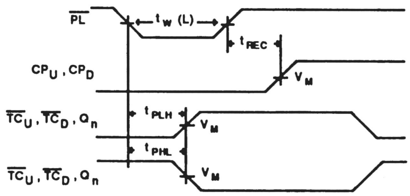
Waveform 2. Propagation Delay, Clock to Terminal Count Output


D_n
TC_U , TC_D , Q_n
V_M
t_PLH
t_PHL

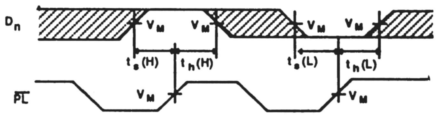
Waveform 3. Propagation Delay, Data to Output


MR
CP_U , CP_D
TC_U , Q_n
TC_D , Q_n
t_w (H)
t_REC
t_PLH
t_PHL
V_M

Waveform 4. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time


PL
CP_U , CP_D
TC_U , TC_D , Q_n
TC_U , TC_D , Q_n
t_w (L)
t_REC
t_PLH
t_PHL
V_M

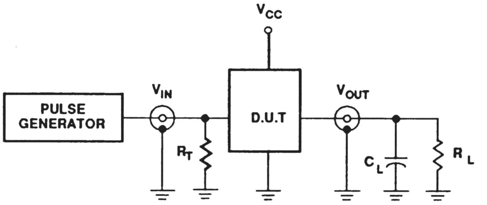
Waveform 5. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time


D_n
PL
V_M
t_s(H)
t_h(H)
t_s(L)
t_h(L)

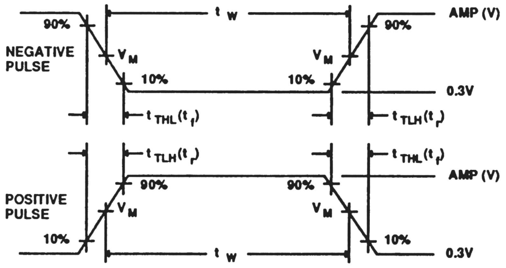
Waveform 6. Data Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.3V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
R_T
D.U.T
V_OUT
C_L
R_L

Test Circuit For Totem-Pole Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
V_M
t_w
t_THL(t_f)
t_TLH(t_r)
AMP (V)
0.3V

$V_M = 1.3V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS240A, 74ALS240A-1
Buffer

Octal Inverter Buffer (3-State)

Product Specification

FEATURES

- **Octal bus interface**
- **3-State buffer outputs sink 24mA and source 15mA**
- **The -1 version sinks 48mA I_{OL} within the ±5% V_{CC} range**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS240A	4.5ns	15mA
74ALS240A-1	4.5ns	15mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74ALS240AN, 74ALS240A-1N
20-Pin Plastic SOL	74ALS240AD, 74ALS240A-1D

DESCRIPTION

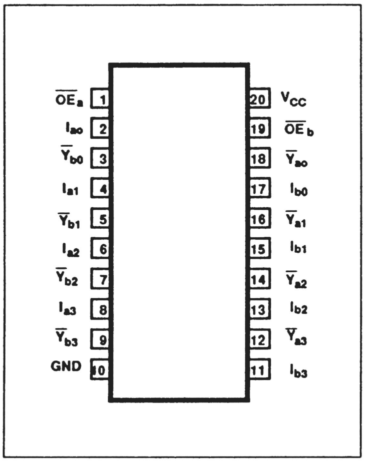
The 74ALS240A is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_a$ and $\overline{OE}_b$, each controlling four of the 3-state outputs. The 74ALS240A-1 sinks 48mA if the V_{CC} is limited to 5.0V ± 0.25V.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}_a$ $\overline{OE}_b$	Output enable inputs (active Low)	1.0/1.0	20µA/0.1mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs	750/240	15mA/24mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs (-1 version)	750/480	15mA/48mA

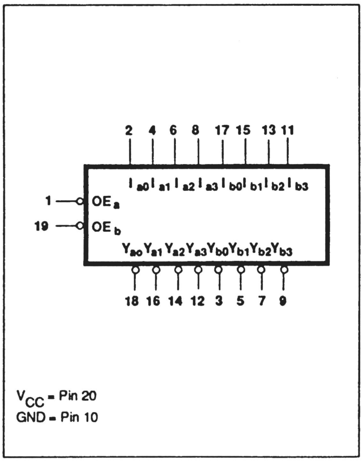
NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION



OEa 1
Ia0 2
Yb0 3
Ia1 4
Yb1 5
Ia2 6
Yb2 7
Ia3 8
Yb3 9
GND 10
20 VCC
19 OEb
18 Ya0
17 Ib0
16 Ya1
15 Ib1
14 Ya2
13 Ib2
12 Ya3
11 Ib3

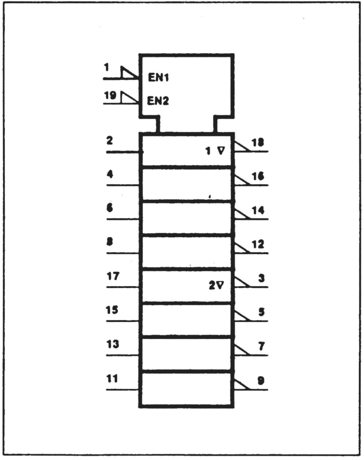
LOGIC SYMBOL



2 4 6 8 17 15 13 11
Ia0 Ia1 Ia2 Ia3 Ib0 Ib1 Ib2 Ib3
1 OEa
19 OEb
Ya0 Ya1 Ya2 Ya3 Yb0 Yb1 Yb2 Yb3
18 16 14 12 3 5 7 9

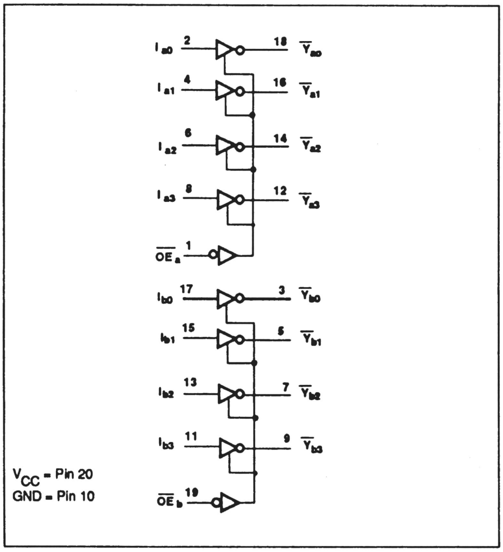
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



1
EN1
19
EN2
2
1 ∇
18
4
16
6
14
8
12
17
2∇
3
15
5
13
7
11
9

LOGIC DIAGRAM


I_{a0} 2
18 $\overline{Y}_{a0}$
I_{a1} 4
16 $\overline{Y}_{a1}$
I_{a2} 6
14 $\overline{Y}_{a2}$
I_{a3} 8
12 $\overline{Y}_{a3}$
$\overline{OE}_a$ 1
I_{b0} 17
3 $\overline{Y}_{b0}$
I_{b1} 15
5 $\overline{Y}_{b1}$
I_{b2} 13
7 $\overline{Y}_{b2}$
I_{b3} 11
9 $\overline{Y}_{b3}$
$\overline{OE}_b$ 19
V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
I_{OUT}	Current applied to output in Low output state	-1 version only	96	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	All versions			24	mA
I_{OL}	Low-level output current	-1 version only			48[1]	mA
T_A	Operating free-air temperature range		0		70	°C

NOTE:

1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ± 5%.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ± 10%	V_{IL} = MAX V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} -2			V
			V_{CC} = MIN		I_{OH} = -3mA	2.4	3.2		V
					I_{OH} = -15mA	2.0			V
V_{OL}	Low-level output voltage	All versions	V_{CC} = MIN	V_{IL} = MAX V_{IH} = MIN	I_{OL} = 12mA		0.25	0.4	V
					I_{OL} = 24mA		0.35	0.5	V
		-1 version	V_{CC} = 4.75V		I_{OL} = 48mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V					-0.1	mA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O= 2.7V					20	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.4V					-20	µA
I_O	Short-circuit output current[3]		V_{CC} = MAX,V_O= 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				2.5	11	mA
		I_{CCL}					19.5	23	mA
		I_{CCZ}					23	30	mA

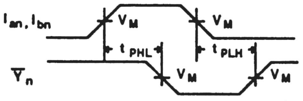
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

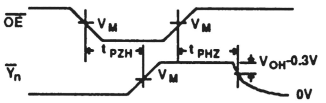
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω Min	 Max	UNIT
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	2.0 2.0	9.0 9.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	2.0 3.0	10.0 12.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	2.0 3.0	10.0 12.0	ns ns

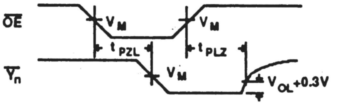
AC WAVEFORMS


I_{an}, I_{bn}
V_M
V_M
t_{PHL}
t_{PLH}
$\overline{Y}_n$
V_M
V_M

Waveform 1. For Inverting Outputs


$\overline{OE}$
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH}-0.3V
$\overline{Y}_n$
V_M
0V

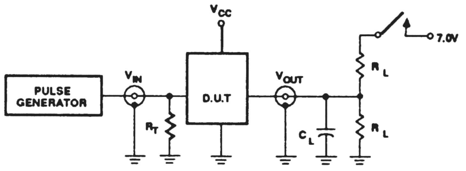
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{OE}$
V_M
V_M
t_{PZL}
t_{PLZ}
$\overline{Y}_n$
V_M
V_{OL}+0.3V

Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.3V.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L
R_L

Test Circuit For 3-State Outputs

SWITCH POSITION

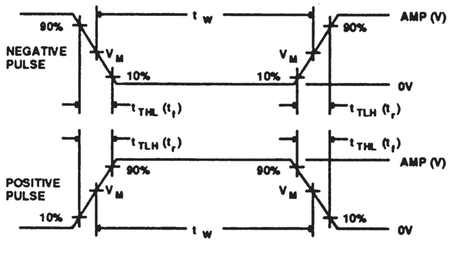
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t_W
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
t_W
0V

V_M = 1.3V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	 Rep. Rate	 t_W	 t_{TLH}	 t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS241A, 74ALS241A-1
Buffer

Octal Buffer (3-State)
Product Specification

FEATURES

- **Octal bus interface**
- **3-State buffer outputs sink 24mA and source 15mA**
- **The -1 version sinks 48mA I_{OL} within the ±5% V_{CC} range**

DESCRIPTION

The 74ALS241A is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_a$ and OE_b, each controlling four of the 3-state outputs. The 74ALS241A-1 sinks 48mA if the V_{CC} is limited to 5.0V ± 0.25V.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS241A	4.5ns	18mA
74ALS241A-1	4.5ns	18mA

ORDERING INFORMATION

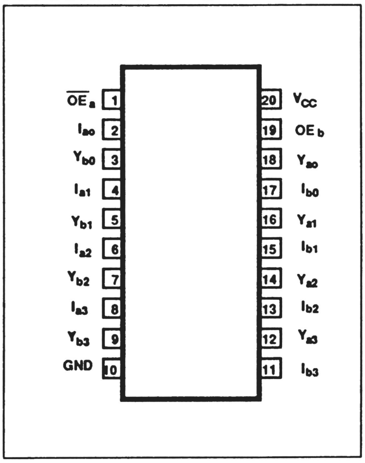
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74ALS241AN, 74ALS241A-1N
20-Pin Plastic SOL	74ALS241AD, 74ALS241A-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}_a$ OE_b	Output enable inputs (active Low)	1.0/1.0	20µA/0.1mA
Y_{an}, Y_{bn}	Data outputs	750/240	15mA/24mA
Y_{an}, Y_{bn}	Data outputs (-1 version)	750/480	15mA48mA

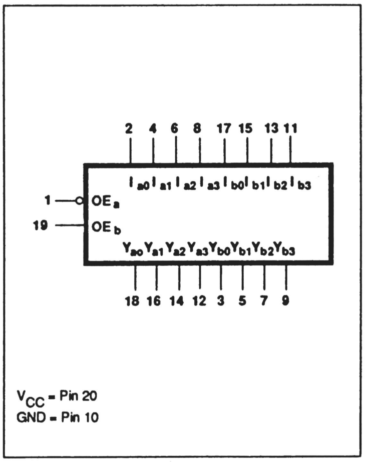
NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION



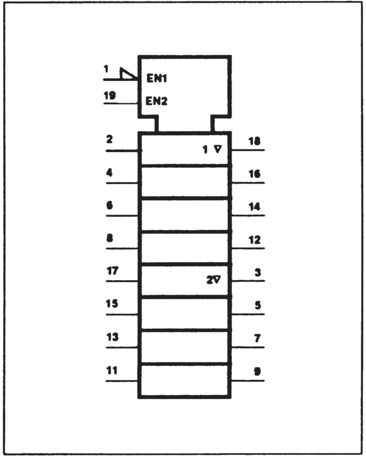
$\overline{OE}_a$ 1
I_{a0} 2
Y_{b0} 3
I_{a1} 4
Y_{b1} 5
I_{a2} 6
Y_{b2} 7
I_{a3} 8
Y_{b3} 9
GND 10
20 V_{CC}
19 OE_b
18 Y_{a0}
17 I_{b0}
16 Y_{a1}
15 I_{b1}
14 Y_{a2}
13 I_{b2}
12 Y_{a3}
11 I_{b3}

LOGIC SYMBOL



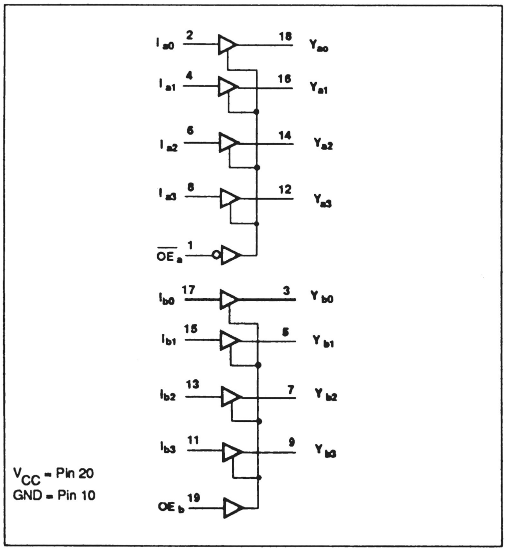
2 4 6 8 17 15 13 11
I_{a0} I_{a1} I_{a2} I_{a3} I_{b0} I_{b1} I_{b2} I_{b3}
1 OE_a
19 OE_b
Y_{a0} Y_{a1} Y_{a2} Y_{a3} Y_{b0} Y_{b1} Y_{b2} Y_{b3}
18 16 14 12 3 5 7 9
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



1 EN1
19 EN2
2 1∇ 18
4 16
6 14
8 12
17 2∇ 3
15 5
13 7
11 9

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
I_{OUT}	Current applied to output in Low output state	-1 version only	96	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	All versions			24	mA
I_{OL}	Low-level output current	-1 version only			48[1]	mA
T_A	Operating free-air temperature range		0		70	°C

NOTES:

1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ± 5%.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ± 10%	V_{IL} = MAX V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} -2			V
			V_{CC} = MIN		I_{OH} = -3mA	2.4	3.2		V
					I_{OH} = -15mA	2.0			V
V_{OL}	Low-level output voltage	All versions	V_{CC} = MIN	V_{IL} = MAX V_{IH} = MIN	I_{OL} = 12mA		0.25	0.4	V
					I_{OL} = 24mA		0.35	0.5	V
		-1 version	V_{CC} = 4.75V		I_{OL} = 48mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V					-0.1	mA
I_{OZH}	Off-state current High level voltage applied		V_{CC} = MAX, V_O = 2.7V					20	µA
I_{OZL}	Off-state current Low-level voltage applied		V_{CC} = MAX, V_O = 0.4V					-20	µA
I_O	Short-circuit output current[3]		V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				7	15	mA
		I_{CCL}					21	26	mA
		I_{CCZ}					25	30	mA

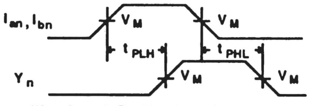
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

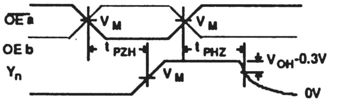
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	1.5 1.5	10.0 10.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	1.0 2.5	10.0 12.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	1.0 2.5	10.0 12.0	ns ns

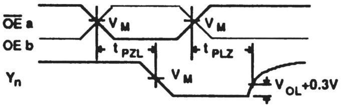
AC WAVEFORMS


I_{an}, I_{bn}
V_M
V_M
t_{PLH}
t_{PHL}
Y_n
V_M
V_M

Waveform 1. For Non-Inverting Outputs


$\overline{OE}$ a
OE b
Y_n
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH}-0.3V
V_M
0V

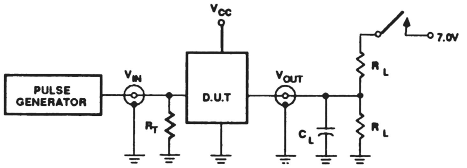
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{OE}$ a
OE b
Y_n
V_M
V_M
t_{PZL}
t_{PLZ}
V_M
V_{OL}+0.3V

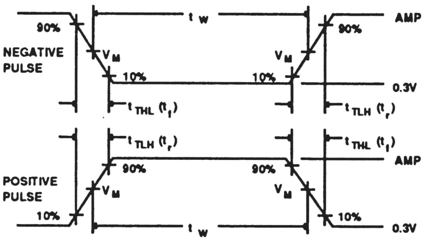
Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.3V.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_T
C_L
R_L
R_L

Test Circuit For 3-State Outputs


NEGATIVE PULSE
90%
V_M
10%
t_W
AMP
90%
V_M
10%
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
POSITIVE PULSE
t_{TLH} (t_r)
t_{THL} (t_f)
90%
90%
AMP
V_M
V_M
10%
10%
t_W
0.3V

V_M = 1.3V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS244A, 74ALS244A-1
Buffer

Octal Buffer (3-State)
Product Specification

FEATURES

- **Octal bus interface**
- **3-State buffer outputs sink 24mA and source 15mA**
- **The -1 version sinks 48mA I_{OL} within the ±5% V_{CC} range**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS244A	4.5ns	17mA
74ALS244A-1	4.5ns	17mA

DESCRIPTION

The 74ALS244A is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_a$ and $\overline{OE}_b$, each controlling four of the 3-state outputs. The 74ALS244A-1 sinks 48mA if the V_{CC} is limited to 5.0V ± 0.25V.

ORDERING INFORMATION

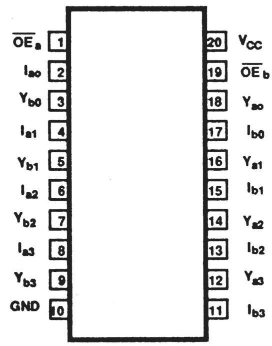
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74ALS244AN, 74ALS244A-1N
20-Pin Plastic SOL	74ALS244AD, 74ALS244A-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}_a$ $\overline{OE}_b$	Output enable inputs (active Low)	1.0/1.0	20µA/0.1mA
Y_{an}, Y_{bn}	Data outputs	750/240	15mA/24mA
Y_{an}, Y_{bn}	Data outputs (-1 version)	750/480	15mA/48mA

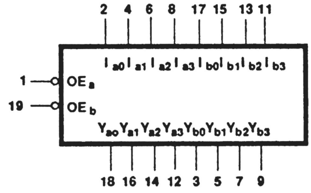
NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION



$\overline{OE}_a$ 1
I_{a0} 2
Y_{b0} 3
I_{a1} 4
Y_{b1} 5
I_{a2} 6
Y_{b2} 7
I_{a3} 8
Y_{b3} 9
GND 10
20 V_{CC}
19 $\overline{OE}_b$
18 Y_{a0}
17 I_{b0}
16 Y_{a1}
15 I_{b1}
14 Y_{a2}
13 I_{b2}
12 Y_{a3}
11 I_{b3}

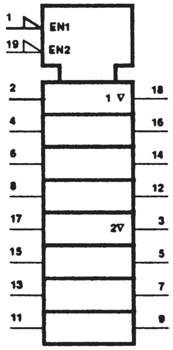
LOGIC SYMBOL



2 4 6 8 17 15 13 11
I_{a0} I_{a1} I_{a2} I_{a3} I_{b0} I_{b1} I_{b2} I_{b3}
1 OE_a
19 OE_b
Y_{a0} Y_{a1} Y_{a2} Y_{a3} Y_{b0} Y_{b1} Y_{b2} Y_{b3}
18 16 14 12 3 5 7 9

V_{CC} = Pin 20
GND = Pin 10

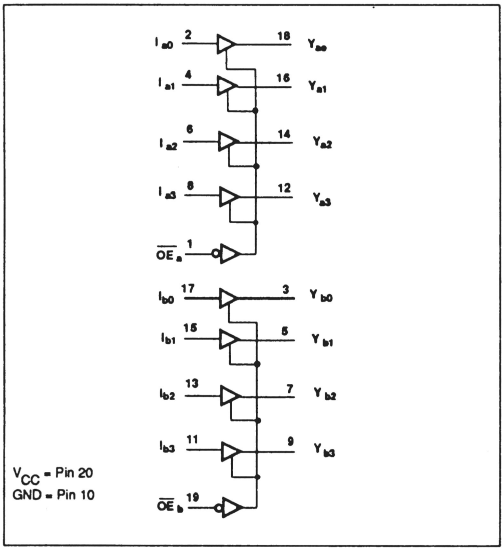
LOGIC SYMBOL (IEEE/IEC)



1
EN1
19
EN2
2
1 ▽
18
4
16
6
14
8
12
17
2▽
3
15
5
13
7
11
9

October 8, 1987

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
I_{OUT}	Current applied to output in Low output state	-1 version only	96	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	All versions			24	mA
I_{OL}	Low-level output current	-1 version only			48[1]	mA
T_A	Operating free-air temperature range		0		70	°C

NOTES:

1. The 48mA limit applies only under the condition of $V_{CC} = 5.0V \pm 5\%$.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ± 10%	V_{IL} = MAX V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} -2			V
			V_{CC} = MIN		I_{OH} = -3mA	2.4	3.2		V
					I_{OH} = -15mA	2.0			V
V_{OL}	Low-level output voltage	All versions	V_{CC} = MIN	V_{IL} = MAX V_{IH} = MIN	I_{OL} = 12mA		0.25	0.4	V
					I_{OL} = 24mA		0.35	0.5	V
		-1 version	V_{CC} = 4.75V		I_{OL} = 48mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V					-0.1	mA
I_{OZH}	Off state output current High-level voltage applied		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_I = 0.4V					-20	µA
I_O	Short circuit current[3]		V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				6.5	15	mA
		I_{CCL}					19.5	24	mA
		I_{CCZ}					25	30	mA

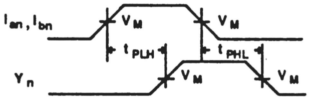
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

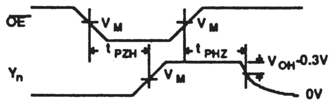
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	1.5 1.5	10.0 10.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	1.0 2.5	10.0 12.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	2.5 2.5	10.0 12.0	ns ns

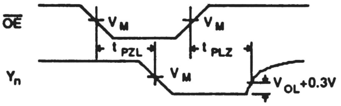
AC WAVEFORMS


I_{an}, I_{bn}
V_M
V_M
t_{PLH}
t_{PHL}
Y_n
V_M
V_M

Waveform 1. For Non-Inverting Outputs


$\overline{OE}$
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH}-0.3V
Y_n
V_M
0V

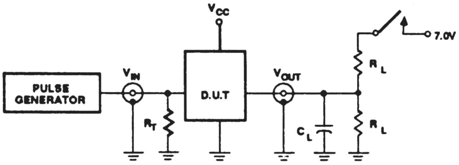
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{OE}$
V_M
V_M
t_{PZL}
t_{PLZ}
Y_n
V_M
V_{OL}+0.3V

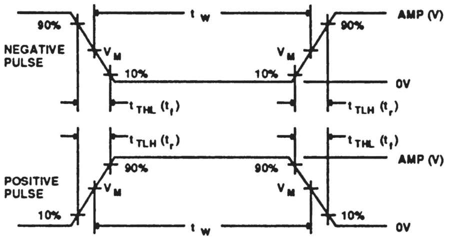
Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.3V.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L
R_L

Test Circuit For 3-State Outputs


NEGATIVE PULSE
90%
V_M
10%
t_w
AMP (V)
0V
t_{THL} (t_f)
t_{TLH} (t_r)
POSITIVE PULSE
90%
V_M
10%
t_w
AMP (V)
0V

V_M = 1.3V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS245A, 74ALS245A-1

Transceivers

Octal Transceivers (3-State)

Product Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-state buffer outputs sink 24mA and source 15mA.**
- **Outputs are placed in high impedance state during power-off conditions**
- **The -1 version sinks 48mA I_{OL} within the ±5% V_{CC} range**

DESCRIPTION

The 74ALS245A is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both transmit and receive directions. The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive(T/$\overline{R}$) input for direction control. The 74ALS245A-1 is the same as the 74ALS245A except that the B port sinks 48 mA within the ±5% V_{CC} range.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS245A 74ALS245A-1	7.0ns	34mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74ALS245AN, 7AL245A-1N
20-Pin Plastic SOL	74ALS245AD, 7AL245A-1D

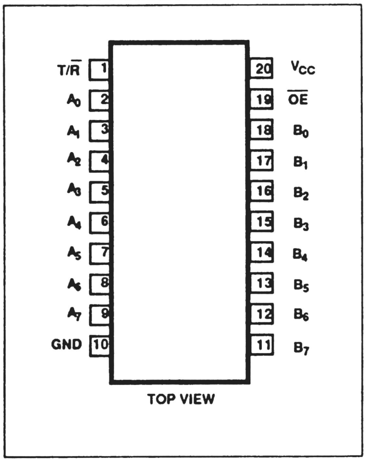
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	1.0/1.0	20μA/0.1mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20μA/0.1mA
T/$\overline{R}$	Transmit/Receive input	1.0/1.0	20μA/0.1mA
A_0- A_7	A port outputs	750/240	15mA/24mA
B_0- B_7	B Port outputs	750/240	15mA/24mA
B_0- B_7	B Port outputs (-1 version)	750/480	15mA/48mA

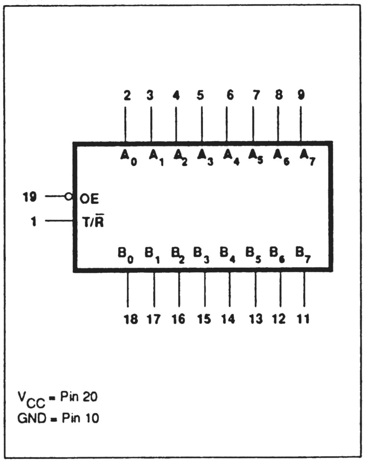
NOTE:

One (1.0) ALS Unit Load is defined as: 20μA in the High state and 0.1mA in the Low state.

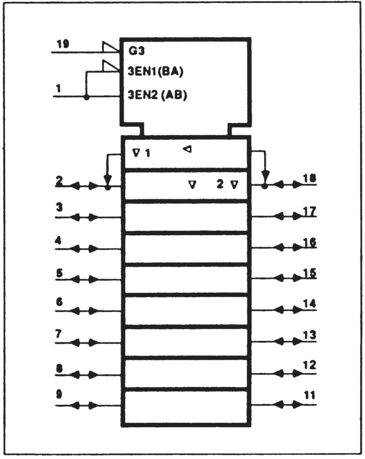
PIN CONFIGURATION


T/R̄ 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
GND 10
20 VCC
19 OE
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
TOP VIEW

LOGIC SYMBOL


2 3 4 5 6 7 8 9
A0 A1 A2 A3 A4 A5 A6 A7
19 OE
1 T/R̄
B0 B1 B2 B3 B4 B5 B6 B7
18 17 16 15 14 13 12 11
VCC = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

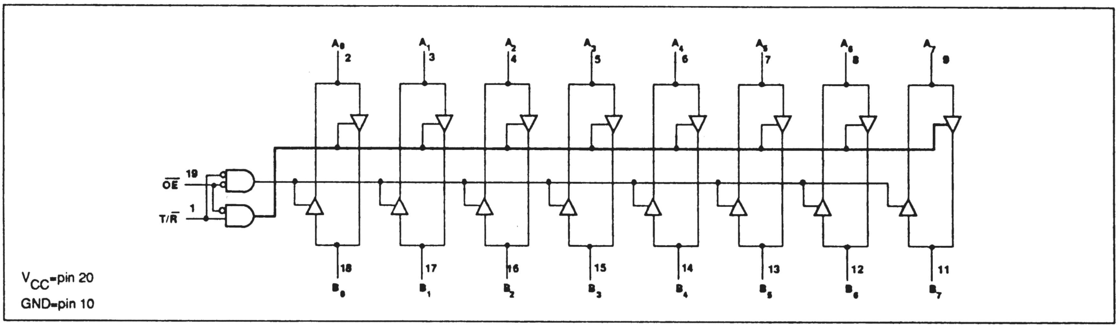

19
1
G3
3EN1(BA)
3EN2 (AB)
▽1 ◁
▽ 2▽
2 3 4 5 6 7 8 9
18 17 16 15 14 13 12 11

FUNCTION TABLE

INTPUTS		OUTPUTS
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version only	96	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version only			48[1]	mA
T_A	Operating free-air temperature range		0		70	°C

NOTE: 1. The 48 mA limit applies only under the condition of V_{CC} = 5.0V±5%.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ± 10%	V_{IL} = MAX V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} -2			V
			V_{CC} = MIN		I_{OH} = -3mA	2.4	3.2		V
					I_{OH} = -15mA	2.0			V
V_{OL}	Low-level output voltage	All versions	V_{CC} = MIN	V_{IL} = MAX V_{IH} = MIN	I_{OL} = 12mA		0.25	0.4	V
					I_{OL} = 24mA		0.35	0.5	V
		-1 version	V_{CC} = 4.75V		I_{OL} = 48mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.5	V
I_I	Input current at maximum input voltage - $\overline{OE}$ or T/$\overline{R}$		V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_I	Input current at maximum input voltage - A or B ports		V_{CC} = MAX, V_I = 5.5V					0.1	mA
I_{IH}	High-level input current[3]		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current[3]		V_{CC} = MAX, V_I = 0.4V					-0.1	mA
I_O	Short-circuit output current[4]		V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				28	45	mA
		I_{CCL}					40	55	mA
		I_{CCZ}					44	58	mA

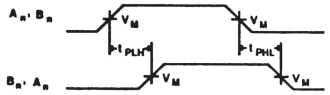
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

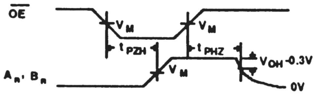
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2 2	10 10	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	3 3	20 20	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	2 4	10 15	ns

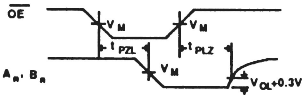
AC WAVEFORMS


A_n, B_n
V_M
t_{PLH}
t_{PHL}
B_n, A_n
V_M

Waveform 1. Propagation Delay For Non-Inverting Output


$\overline{OE}$
V_M
t_{PZH}
t_{PHZ}
V_{OH}-0.3V
A_n, B_n
0V

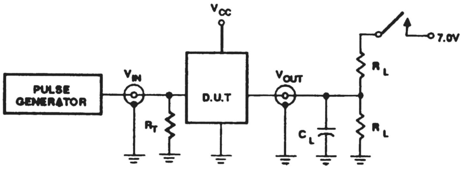
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{OE}$
V_M
t_{PZL}
t_{PLZ}
A_n, B_n
V_{OL}+0.3V

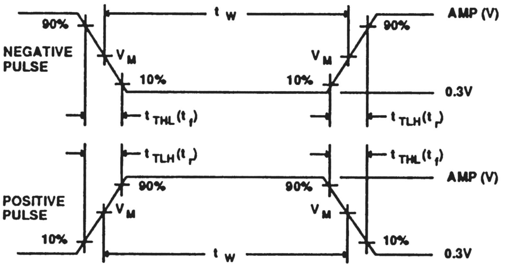
Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.3V.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_L
R_T
C_L
R_L

Test Circuit For 3-State Outputs


90%
NEGATIVE PULSE
t_W
AMP (V)
V_M
10%
0.3V
$t_{THL}(t_f)$
$t_{TLH}(t_r)$
POSITIVE PULSE
90%
AMP (V)
10%
0.3V

V_M = 1.3V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS251
Multiplexer

74ALS251 8-Input Multiplexer (3-State)
Preliminary Specification

FEATURES

- **8-to-1 multiplexing**
- **On chip decoding**
- **Multifunction capability**
- **Inverting and Non-Inverting outputs**
- **Both outputs are 3-state for further multiplexer expansion**

DESCRIPTION

The 74ALS251 is a logic implementation of a single 8-position switch with the switch position controlled by the state of three Select (S_0,S_1,S_2) inputs. True(Y) and complementary ($\overline{Y}$) outputs are both provided. The output Enable ($\overline{OE}$) is active Low. When $\overline{OE}$ is High, both outputs are in high impedance state, allowing multiple output connections to a common bus without driving nor loading the bus significantly. When the outputs of more than one device are tied together, the user must ensure that there is no overlap in the active Low portion of the output enable voltages in order to avoid high currents that could exceed the maximum current rating.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS251	12ns	7.5mA

ORDERING INFORMATION

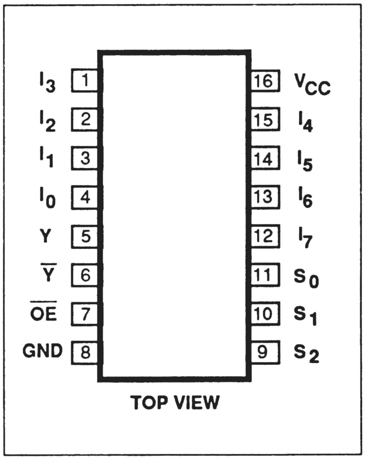
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74ALS251N
16-Pin Plastic SO	N74ALS251D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0- I_7	Data inputs	1.0/1.0	20µA/0.1mA
S_0- S_2	Select inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.1mA
Y, $\overline{Y}$	Data outputs	130/240	2.6mA/24mA

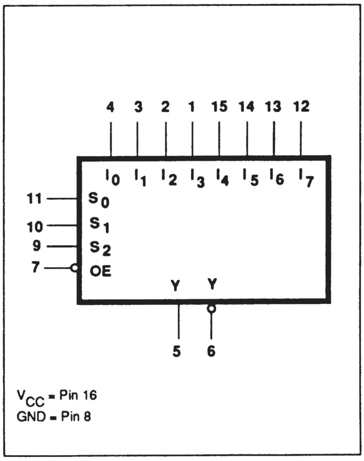
NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



I_3 1
I_2 2
I_1 3
I_0 4
Y 5
$\overline{Y}$ 6
$\overline{OE}$ 7
GND 8
16 V_{CC}
15 I_4
14 I_5
13 I_6
12 I_7
11 S_0
10 S_1
9 S_2
TOP VIEW

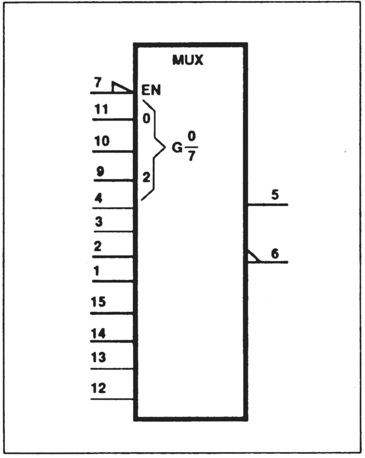
LOGIC SYMBOL



4 3 2 1 15 14 13 12
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7
11 S_0
10 S_1
9 S_2
7 OE
Y Y
5 6

V_{CC} = Pin 16
GND = Pin 8

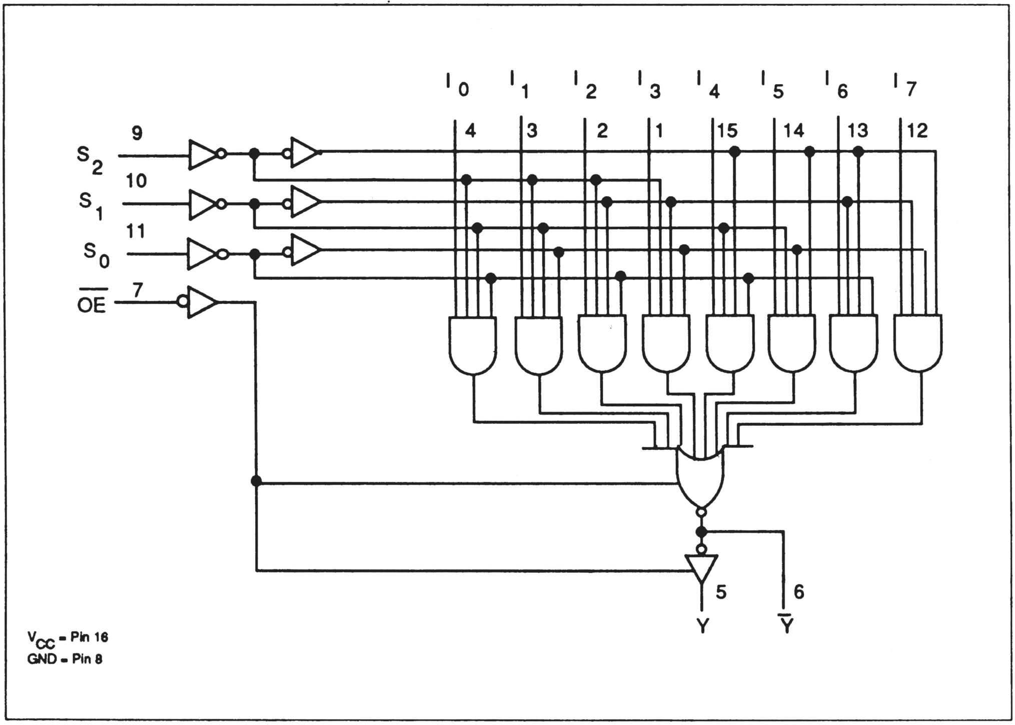
LOGIC SYMBOL(IEEE/IEC)



MUX
7 EN
11 0
10 G $\frac{0}{7}$
9 2
4
3
2
1
15
14
13
12
5
6

August 1988

LOGIC DIAGRAM


I0
I1
I2
I3
I4
I5
I6
I7
4
3
2
1
15
14
13
12
S2
9
S1
10
S0
11
OE
7
5
6
Y
Ȳ
V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	Z	Z
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	**Nom**	**Max**	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	**Typ**[2]	**Max**	
V_{OH}	High-level output voltage		$V_{CC}\pm10\%$	V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} - 2			V
			V_{CC} = MIN		I_{OH} = -2.6mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA			0.25	0.4	V
				I_{OL} = 24mA			0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.5	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V					-0.1	mA
I_O[3]	Output current		V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	I_{CC}	V_{CC} = MAX				7	10	mA
		I_{CCZ}					9.4	14	mA

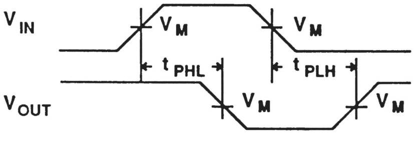
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

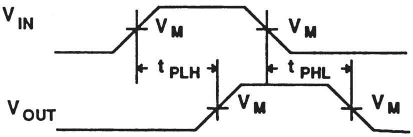
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	Waveform 2	2 3	10 15	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	Waveform 1	3 3	15 15	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	Waveform 1,2	5 8	18 24	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	Waveform 1,2	8 7	24 23	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Y	Waveform 3 Waveform 4	3 3	15 15	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Y	Waveform 3 Waveform 4	3 3	15 15	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{Y}$	Waveform 3 Waveform 4	2 1	10 10	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to $\overline{Y}$	Waveform 3 Waveform 4	2 1	10 10	ns ns

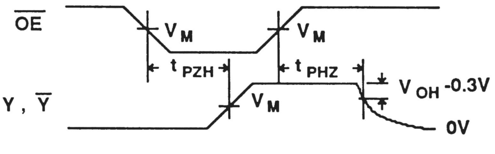
AC WAVEFORMS


V_{IN}
V_M
V_M
t_{PHL}
t_{PLH}
V_{OUT}
V_M
V_M

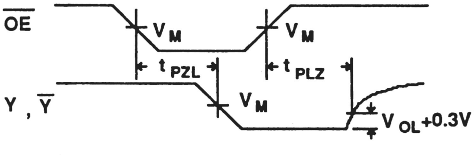
Waveform 1. For Inverting Outputs


V_{IN}
V_M
V_M
t_{PLH}
t_{PHL}
V_{OUT}
V_M
V_M

Waveform 2. For Non-Inverting Outputs

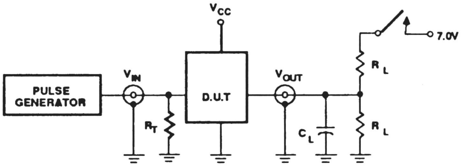

$\overline{OE}$
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH} -0.3V
Y , $\overline{Y}$
V_M
0V

Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{OE}$
V_M
V_M
t_{PZL}
t_{PLZ}
Y , $\overline{Y}$
V_M
V_{OL}+0.3V

Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

TEST CIRCUIT AND WAVEFORMS


V_CC
7.0V
R_L
PULSE GENERATOR
V_IN
D.U.T
V_OUT
R_T
C_L
R_L

Test Circuit For 3-State Outputs

SWITCH POSITION

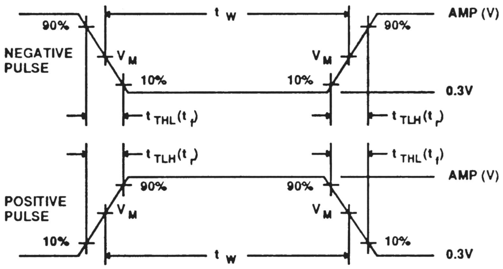
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t_W
AMP (V)
90%
90%
NEGATIVE PULSE
V_M
V_M
10%
10%
0.3V
t_THL(t_f)
t_TLH(t_r)
t_TLH(t_r)
t_THL(t_f)
AMP (V)
90%
90%
POSITIVE PULSE
V_M
V_M
10%
10%
0.3V
t_W

$V_M = 1.3V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	**Rep. Rate**	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS253
Multiplexer

Dual 4-Input Multiplexer (3-State)

Preliminary Specification

FEATURES

- **3-state outputs for bus interface and multiplex expansion**
- **Common select inputs**
- **Separate Output Enable inputs**

DESCRIPTION

The 74ALS253 has two identical 4-input multiplexers with 3-state outputs which select two bits from four sources by using common select inputs (S_0,S_1). When the individual Output Enable ($\overline{OE}_a$,$\overline{OE}_b$) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance (Z) state.

The 74ALS253 is the logic implementation of a 2-pole,4-position switch being determined by the logic levels supplied to the common select inputs.

To avoid exceeding the maximum current ratings when the outputs of the 3-state devices are tied together, all but one device must be in the high-impedance state. Therefore, only one Output Enable must be active at a time.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS253	7ns	7mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74ALS253N
16-Pin Plastic SO	N74ALS253D

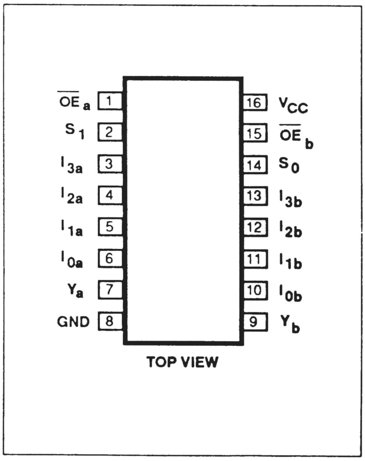
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}- I_{3a}	Port A data inputs	1.0/1.0	20μA/0.1mA
I_{0b}- I_{3b}	Port B data inputs	1.0/1.0	20μA/0.1mA
S_0- S_2	Common Select inputs	1.0/1.0	20μA/0.1mA
$\overline{OE}_a$	Port A output enable input (active Low)	1.0/1.0	20μA/0.1mA
$\overline{OE}_b$	Port b output enable input (active Low)	1.0/1.0	20μA/0.1mA
Y_a, Y_b	3-state outputs	130/240	2.6mA/24mA

NOTE:

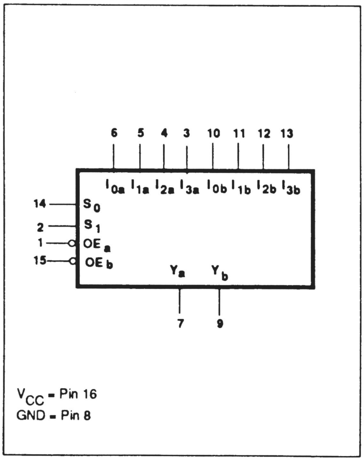
One (1.0) ALS Unit Load is defined as: 20μA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION



$\overline{OE}_a$ 1
S_1 2
I_{3a} 3
I_{2a} 4
I_{1a} 5
I_{0a} 6
Y_a 7
GND 8
16 V_{CC}
15 $\overline{OE}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 Y_b
TOP VIEW

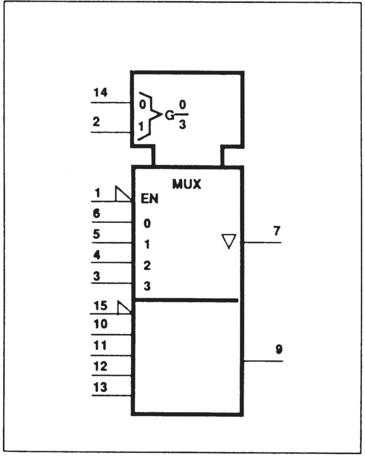
LOGIC SYMBOL



6 5 4 3 10 11 12 13
I_{0a} I_{1a} I_{2a} I_{3a} I_{0b} I_{1b} I_{2b} I_{3b}
14 S_0
2 S_1
1 OE_a
15 OE_b
Y_a Y_b
7 9

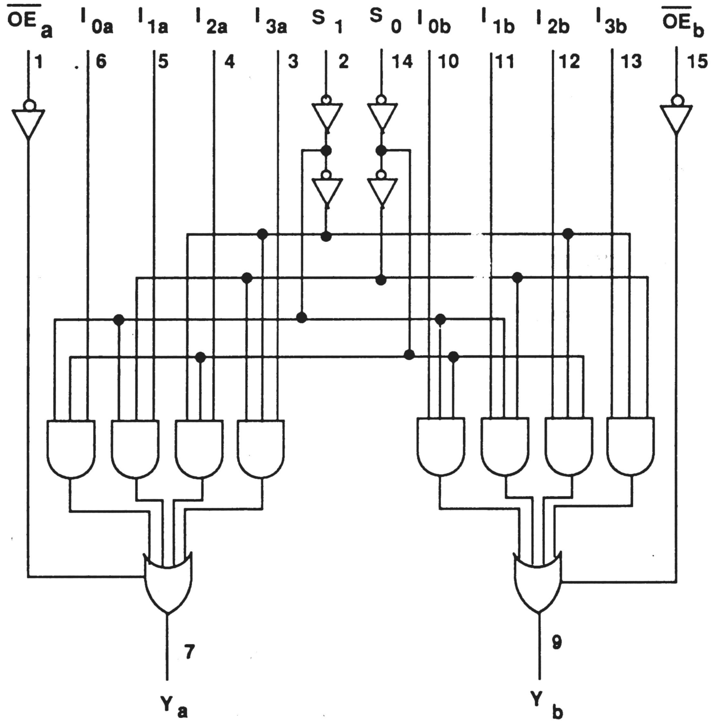
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



14
2
0
1
G $\frac{0}{3}$
MUX
1 EN
6 0
5 1
4 2
3 3
7
15
10
11
12
13
9

LOGIC DIAGRAM


$\overline{OE}_a$
I_{0a}
I_{1a}
I_{2a}
I_{3a}
S_1
S_0
I_{0b}
I_{1b}
I_{2b}
I_{3b}
$\overline{OE}_b$
1
6
5
4
3
2
14
10
11
12
13
15
7
9
Y_a
Y_b

V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC}±10%	V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} - 2			V
			V_{CC} = MIN		I_{OH} = -2.6mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA			0.25	0.4	V
				I_{OL} = 24mA			0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.5	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V					-0.1	mA
I_O[3]	Output current		V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	I_{CC}	V_{CC} = MAX				6.5	12	mA
		I_{CCZ}					7.5	14	mA

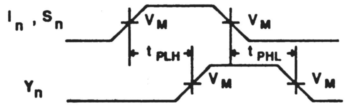
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

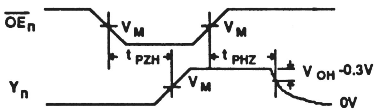
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	2 3	10 14	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	Waveform 1	5 5	21 21	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level	Waveform 2 Waveform 3	3 4	14 16	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level	Waveform 2 Waveform 3	2 2	10 14	ns

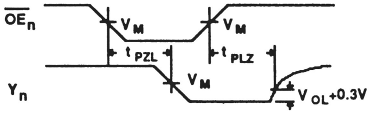
AC WAVEFORMS


I_n, S_n
V_M
V_M
t_{PLH}
t_{PHL}
Y_n
V_M
V_M

Waveform 1. Propagation Delay, Data and Select to Output


$\overline{OE}_n$
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH} -0.3V
Y_n
V_M
0V

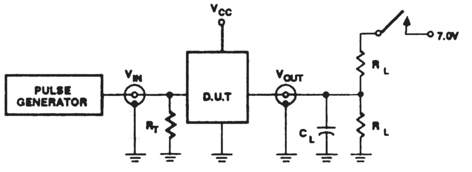
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{OE}_n$
V_M
V_M
t_{PZL}
t_{PLZ}
Y_n
V_M
V_{OL}+0.3V

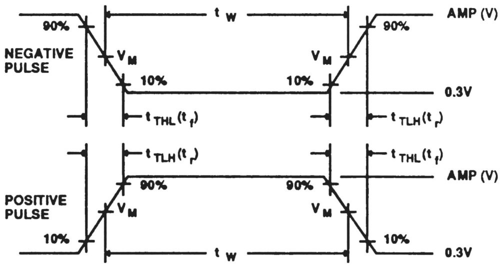
Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.3V.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
R_L
R_T
C_L
R_L

Test Circuit For 3-State Outputs


NEGATIVE PULSE
90%
t_W
AMP (V)
90%
V_M
V_M
10%
10%
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
t_{TLH} (t_r)
t_{THL} (t_f)
AMP (V)
POSITIVE PULSE
90%
90%
V_M
V_M
10%
10%
t_W
0.3V

V_M = 1.3V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS257, 74ALS258
Data Selectors/Multiplexers

74ALS257 Quad 2-Input Data Selector/Multiplexer, Non-Inverting (3-state)
74ALS258 Quad 2-Input Data Selector/Multiplexer, Inverting (3-state)
Product Specification

DESCRIPTION

The 74ALS257 is a Quad 2-input multiplexer which selects 4 bits of data from one of two sources under the control of a common Select input (S). The Output Enable input ($\overline{OE}$) is active when Low. When $\overline{OE}$ is High, all of the outputs (Y_n) are forced to a high impedance state (3-state) regardless of all other input conditions.

Moving data from two registers to a common output bus is a typical use of the 74ALS257. The state of the Select input determines the particular register from which the data comes.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The 74ALS258 is similar but has inverting outputs ($\overline{Y}_n$).

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS257	7.0ns	7mA
74ALS258	7.0ns	7mA

ORDERING INFORMATION

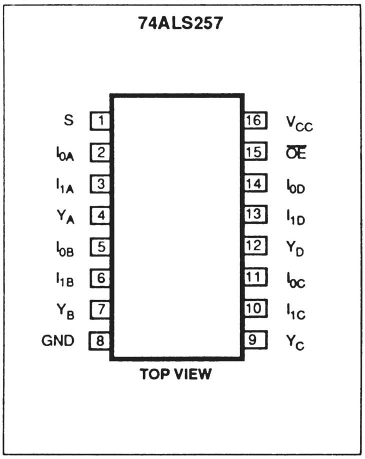
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-pin Plastic DIP	74ALS257N, 74ALS258N
20-pin Plastic SO	74ALS257D, 74ALS258D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

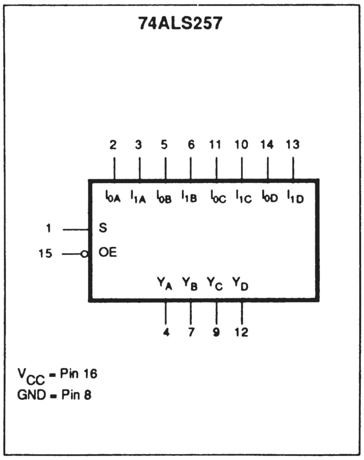
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{nA}, I_{nB}, I_{nC}, I_{nD}	Data inputs	1.0/1.0	20µA/0.1mA
S	Select input	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Output Enable input	1.0/1.0	20µA/0.1mA
Y_A - Y_D, $\overline{Y}_A$ - $\overline{Y}_D$	Data outputs	20/240	0.4mA/24mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

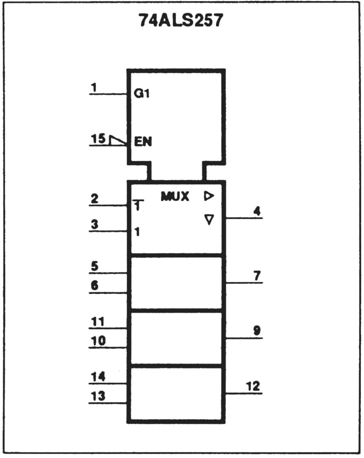

74ALS257
S 1
I0A 2
I1A 3
YA 4
I0B 5
I1B 6
YB 7
GND 8
16 VCC
15 OE
14 I0D
13 I1D
12 YD
11 I0C
10 I1C
9 YC
TOP VIEW

LOGIC SYMBOL

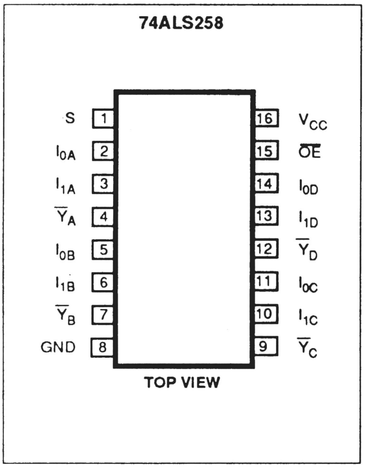

74ALS257
2 3 5 6 11 10 14 13
I0A I1A I0B I1B I0C I1C I0D I1D
1 S
15 OE
YA YB YC YD
4 7 9 12

V_{CC} = Pin 16
GND = Pin 8

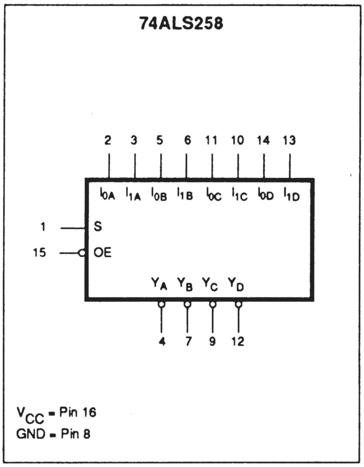
LOGIC SYMBOL (IEEE/IEC)


74ALS257
1 G1
15 EN
MUX
2
3
1
4
5
6
7
11
10
9
14
13
12

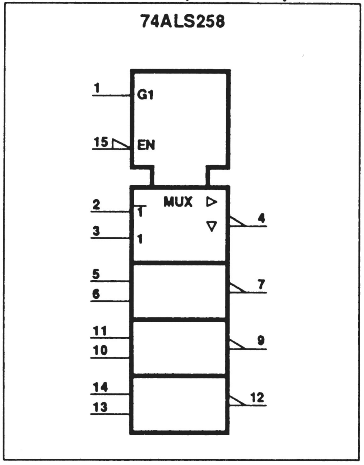
PIN CONFIGURATION


74ALS258
S 1
I_{0A} 2
I_{1A} 3
$\overline{Y}_A$ 4
I_{0B} 5
I_{1B} 6
$\overline{Y}_B$ 7
GND 8
16 V_{CC}
15 $\overline{OE}$
14 I_{0D}
13 I_{1D}
12 $\overline{Y}_D$
11 I_{0C}
10 I_{1C}
9 $\overline{Y}_C$
TOP VIEW

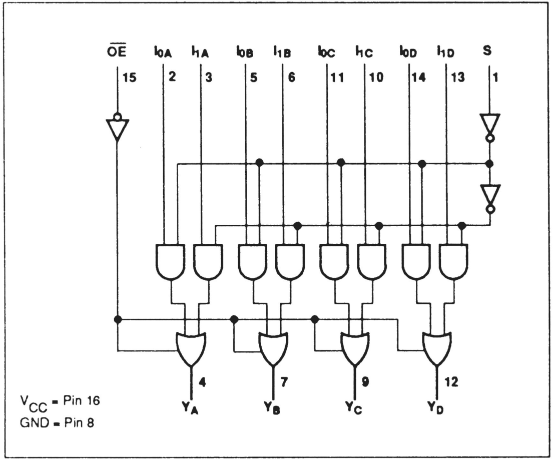
LOGIC SYMBOL


74ALS258
2 3 5 6 11 10 14 13
I_{0A} I_{1A} I_{0B} I_{1B} I_{0C} I_{1C} I_{0D} I_{1D}
1 S
15 OE
Y_A Y_B Y_C Y_D
4 7 9 12
V_{CC} = Pin 16
GND = Pin 8

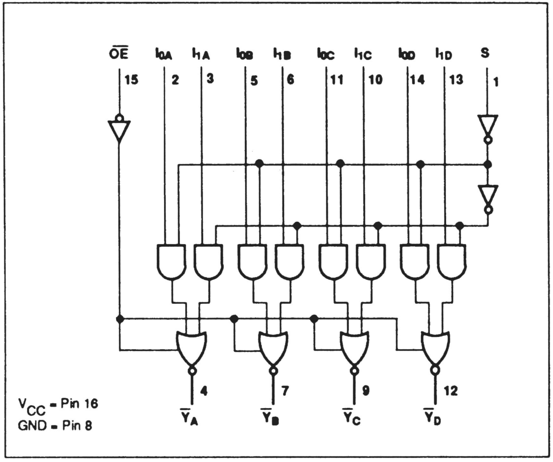
LOGIC SYMBOL (IEEE/IEC)


74ALS258
1 G1
15 EN
MUX
2 $\overline{1}$
3 1
4
5
6
7
11
10
9
14
13
12

LOGIC DIAGRAM, 74ALS257


$\overline{OE}$ I_{0A} I_{1A} I_{0B} I_{1B} I_{0C} I_{1C} I_{0D} I_{1D} S
15 2 3 5 6 11 10 14 13 1
4 7 9 12
Y_A Y_B Y_C Y_D
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM, 74ALS258


$\overline{OE}$ I_{0A} I_{1A} I_{0B} I_{1B} I_{0C} I_{1C} I_{0D} I_{1D} S
15 2 3 5 6 11 10 14 13 1
4 7 9 12
$\overline{Y}_A$ $\overline{Y}_B$ $\overline{Y}_C$ $\overline{Y}_D$
V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_{0n}	I_{1n}	Y_n
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_{0n}	I_{1n}	$\overline{Y}_n$
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC}-2			V
					I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.4	V
					I_{OL} = 24mA		0.35	0.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.4V				-0.1	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				20	μA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.4V				-20	μA
I_O[3]	Output current			V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	74ALS257	I_{CCH}	V_{CC} = MAX			3	6	mA
			I_{CCL}				8	12	mA
			I_{CCZ}				9	14	mA
		74ALS258	I_{CCH}	V_{CC} = MAX			2.5	4	mA
			I_{CCL}				7	11	mA
			I_{CCZ}				9	13	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

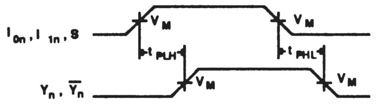
AC ELECTRICAL CHARACTERISTICS for 74ALS257

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{0n} or I_{1n} to Y_n	Waveform 1	2.0 2.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Y	Waveform 1, 2	4.0 4.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Y_n	Waveform 3	3.0 4.0	11.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Y_n	Waveform 4	2.0 5.0	9.0 12.0	ns

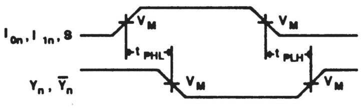
AC ELECTRICAL CHARACTERISTICS for 74ALS258

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay I_{0n} or I_{1n} to $\overline{Y}_n$	Waveform 2	2.0 2.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$	Waveform 1, 2	4.0 4.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{Y}_n$	Waveform 3	3.0 4.0	11.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to $\overline{Y}_n$	Waveform 4	2.0 5.0	9.0 12.0	ns

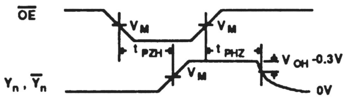
AC WAVEFORMS


I0n, I1n, S
VM
tPLH
tPHL
Yn, Ȳn
VM

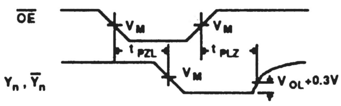
Waveform 1. Propagation Delay For Data And Select To Output


I0n, I1n, S
VM
tPHL
tPLH
Yn, Ȳn
VM

Waveform 2. Propagation Delay For Data And Select To Output


OE
VM
tPZH
tPHZ
VOH -0.3V
Yn, Ȳn
VM
0V

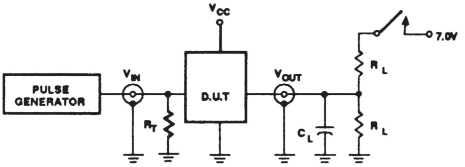
Waveform 3. Propagation Delay For Output Enable To Output


OE
VM
tPZL
tPLZ
Yn, Ȳn
VM
VOL+0.3V

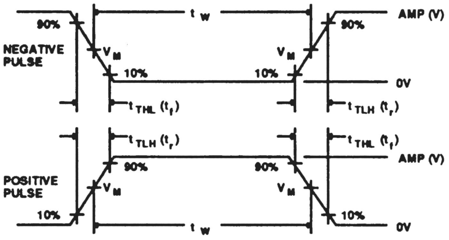
Waveform 4. Propagation Delay For Output Enable To Output

V_M = 1.3V

TEST CIRCUIT AND WAVEFORMS


VCC
7.0V
PULSE GENERATOR
VIN
D.U.T
VOUT
RL
RT
CL
RL

Test Circuit For 3-State Outputs


tW
AMP (V)
90%
NEGATIVE PULSE
VM
10%
0V
tTHL (tf)
tTLH (tr)
POSITIVE PULSE
AMP (V)
90%
VM
10%
0V
tW

V_M = 1.3V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS273
Flip-Flop

Octal D Flip-Flop
Preliminary Specification

FEATURES

- **Eight edge-triggered D-type flip-flops**
- **Buffered common clock**
- **Buffered asynchronous Master Reset**
- **See 'ALS377 for clock enable version**
- **See 'ALS373 for transparent latch version**
- **See 'ALS374 for 3-state version**

TYPE	TYPICAL fMAX	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS273	50MHz	15mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
20-Pin Plastic DIP	N74ALS273N
20-Pin Plastic SOL	N74ALS273D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.1mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.1mA
Q_0 - Q_7	3-State outputs	130/240	2.6mA/24mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

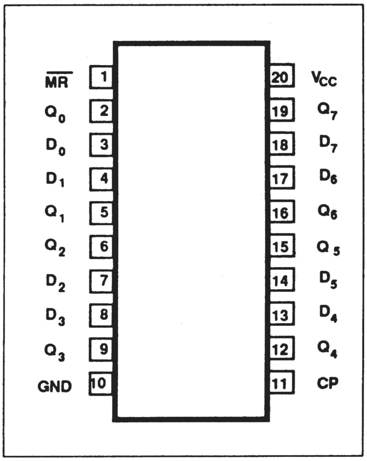
DESCRIPTION

The 74ALS273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

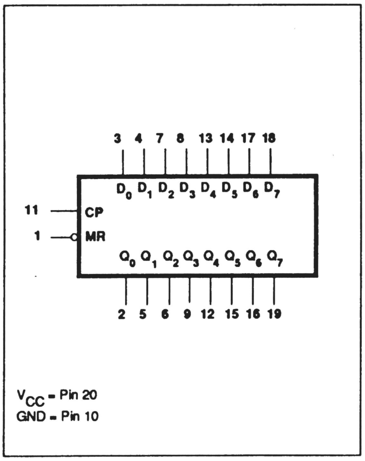
All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common to all flip-flops.

PIN CONFIGURATION



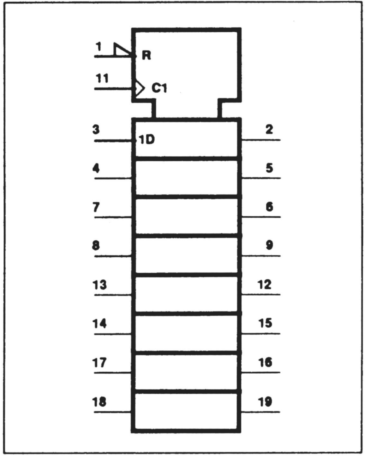
$\overline{MR}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 CP

LOGIC SYMBOL



3 4 7 8 13 14 17 18
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 CP
1 MR
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
2 5 6 9 12 15 16 19
V_{CC} = Pin 20
GND = Pin 10

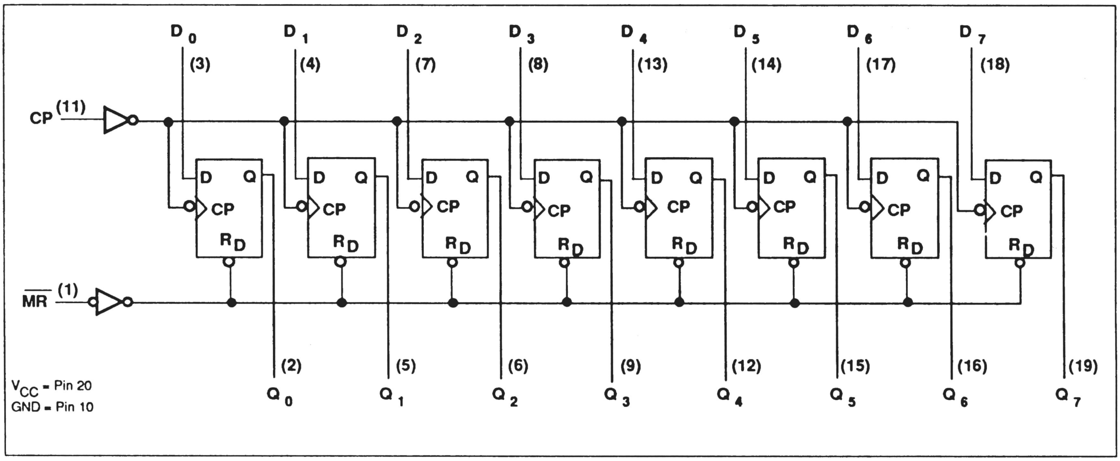
LOGIC SYMBOL(IEEE/IEC)



1 R
11 C1
3 1D 2
4 5
7 6
8 9
13 12
14 15
17 16
18 19

July 1988

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	D_n	Q_0 - Q_7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC}±10%	V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} - 2			V
			V_{CC} = MIN		I_{OH} = -2.6mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA			0.25	0.4	V
				I_{OL} = 24mA			0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.5	V
I_I	Input clamp current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V					-0.1	mA
I_O[3]	Output current		V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				11	20	mA
		I_{CCL}					19	29	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current,I_{OS}.

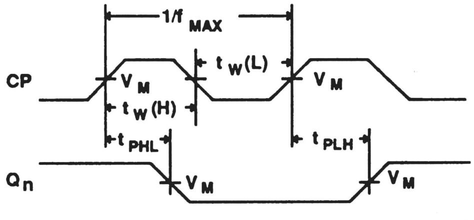
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	35		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n	Waveform 1	2 3	12 15	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4	18	ns

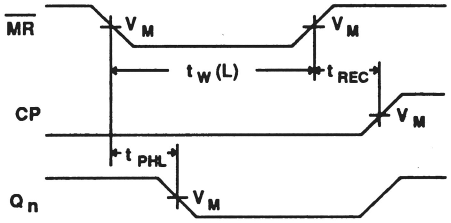
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	10 10		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	14 14		ns
$t_w(L)$	Master Reset Pulse width, Low	Waveform 2	10		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	15		ns

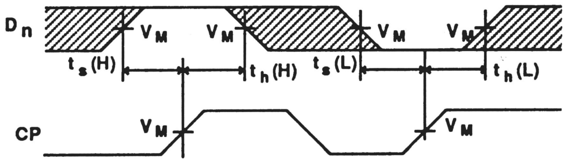
AC WAVEFORMS


1/f MAX
CP
t W(L)
V M
t W(H)
t PHL
t PLH
Q n
V M

Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


MR
V M
t W (L)
t REC
CP
t PHL
Q n

Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

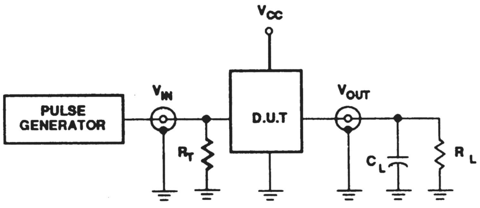

D n
V M
t s (H)
t h (H)
t s (L)
t h (L)
CP

Waveform 3. Data Setup And Hold Times

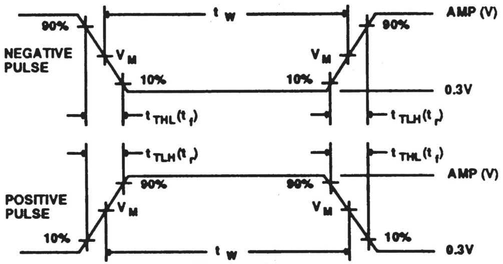
NOTE: For all waveforms, $V_M = 1.3V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V CC
PULSE GENERATOR
V IN
R T
D.U.T
V OUT
C L
R L

Test Circuit For Totem-Pole Outputs


t w
AMP (V)
90%
NEGATIVE PULSE
V M
10%
0.3V
t THL (t f)
t TLH (t r)
POSITIVE PULSE
AMP (V)
90%
10%
0.3V

$V_M = 1.3V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS373, 74ALS374
Latch/Flip-Flop

74ALS373 Octal Transparent Latch (3-State)
74ALS374 Octal D Flip-Flop (3-State)
Product Specification

FEATURES

- **8-bit transparent latch-'ALS373**
- **8-bit positive edge triggered register-'ALS374**
- **3-State Output buffers**
- **Common 3-state Output Enable**
- **Independent register and 3-state buffer operation**

DESCRIPTION

The 74ALS373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS373	6.0ns	14mA
74ALS374	6.0ns	17mA

ORDERING INFORMATION

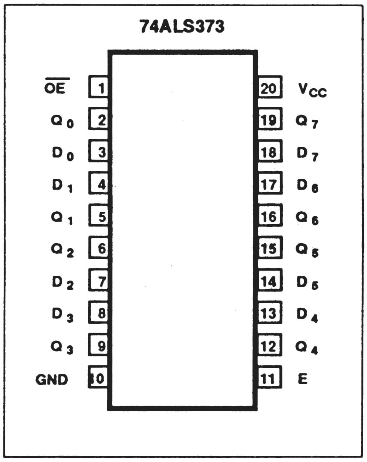
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74ALS373N, 74ALS374N
20-Pin Plastic SOL	74ALS373D, 74ALS374D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

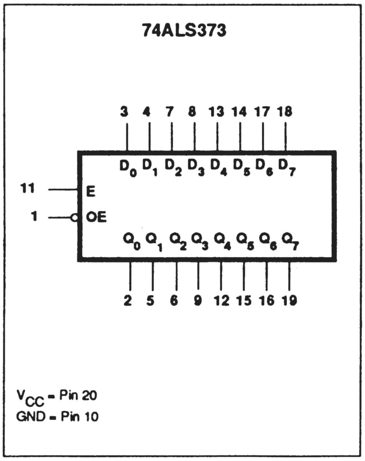
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.1mA
E ('ALS373)	Latch enable input (active High)	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.1mA
CP ('ALS374)	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.1mA
Q_0 - Q_7	3-State outputs	130/240	2.6mA/24mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

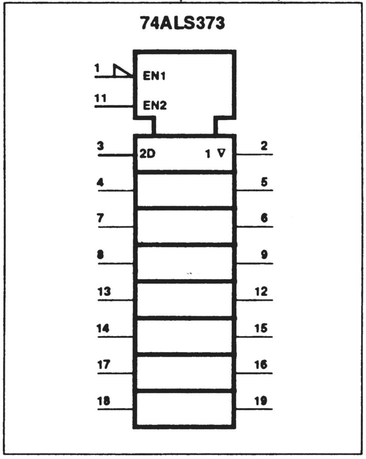

74ALS373
$\overline{OE}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 E

LOGIC SYMBOL

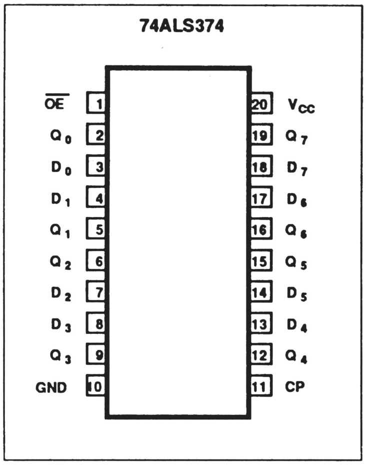

74ALS373
3 4 7 8 13 14 17 18
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 E
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
2 5 6 9 12 15 16 19

V_{CC} = Pin 20
GND = Pin 10

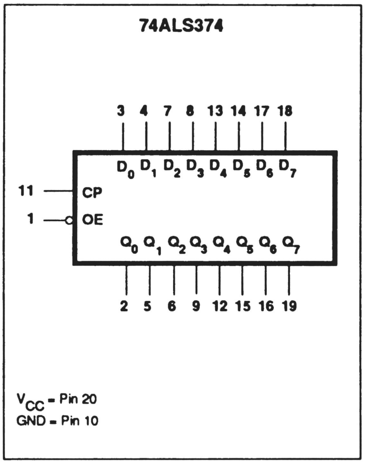
LOGIC SYMBOL(IEEE/IEC)


74ALS373
1
EN1
11
EN2
3
2D
1 ∇
2
4
5
7
6
8
9
13
12
14
15
17
16
18
19

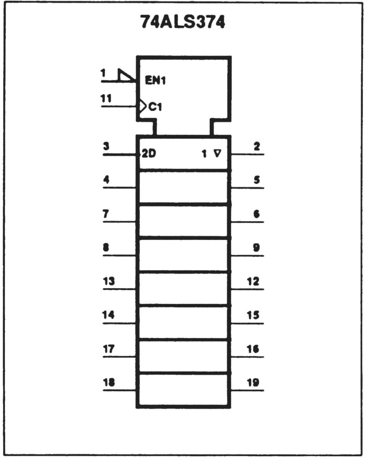
PIN CONFIGURATION


74ALS374
OE 1
Q0 2
D0 3
D1 4
Q1 5
Q2 6
D2 7
D3 8
Q3 9
GND 10
20 VCC
19 Q7
18 D7
17 D6
16 Q6
15 Q5
14 D5
13 D4
12 Q4
11 CP

LOGIC SYMBOL


74ALS374
3 4 7 8 13 14 17 18
D0 D1 D2 D3 D4 D5 D6 D7
11 CP
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
2 5 6 9 12 15 16 19
VCC = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)


74ALS374
1 EN1
11 C1
3 2D 1 ∇ 2
4 5
7 6
8 9
13 12
14 15
17 16
18 19

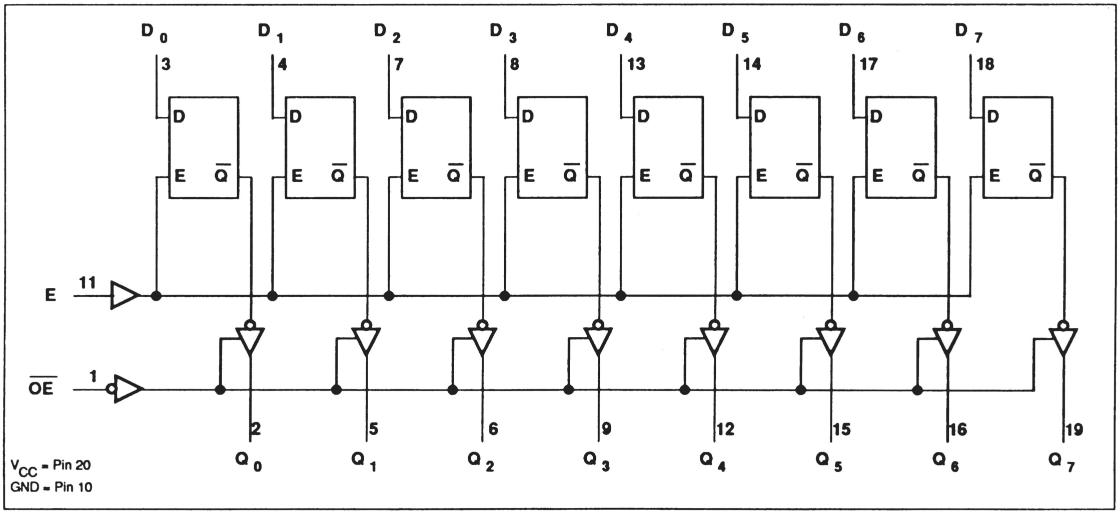
in high impedance "off" state, which means they will neither drive nor load the bus.

The 'ALS374 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

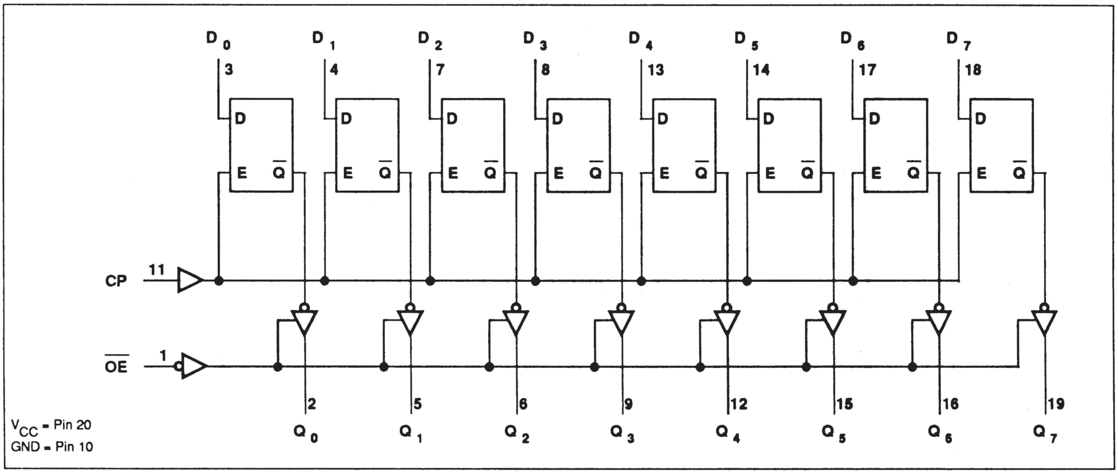
The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 74ALS373


D0 3
D1 4
D2 7
D3 8
D4 13
D5 14
D6 17
D7 18
D
E Q̄
E 11
OE 1
2 Q0
5 Q1
6 Q2
9 Q3
12 Q4
15 Q5
16 Q6
19 Q7
VCC = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 74ALS374



FUNCTION TABLE, 74ALS373

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	Q_0 - Q_7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	D_n	D_n	Z	

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 74ALS374

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↑̸	X	NC	NC	Hold
H	↨	X	NC	Z	Disable outputs
H	↑	D_n	D_n	Z	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↑̸ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC}-2			V
				V_{CC}= MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN	I_{OL} = 12mA		0.25	0.4	V
					I_{OL} = 24mA		0.35	0.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.5	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	74ALS373		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
		74ALS374						-0.2	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				20	μA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.4V				-20	μA
I_O	Output current[3]			V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	74ALS373	V_{CC} = MAX			7	16	mA
		I_{CCL}					14	25	mA
		I_{CCZ}					17	27	mA
		I_{CCH}	74ALS374	V_{CC} = MAX			11	19	mA
		I_{CCL}					19	28	mA
		I_{CCZ}					20	31	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}

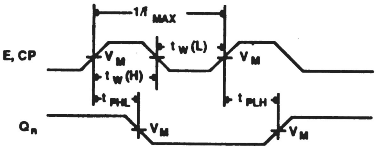
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
				Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74ALS373	Waveform 2	2.0 2.0	12.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 1	3.0 3.0	14.0 14.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.0 3.0	14.0 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	2.0 2.0	10.0 12.0	ns
f_{MAX}	Maximum Clock frequency	74ALS374	Waveform 1	50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	3.0 4.0	12.0 14.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	3.0 3.0	14.0 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	2.0 3.0	10.0 12.0	ns

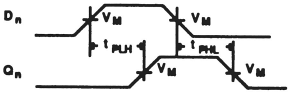
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
				Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	74ALS373	Waveform 3	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E		Waveform 3	6.0 6.0		ns
$t_w(H)$	E Pulse width, High		Waveform 1	10.0		ns
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	74ALS374	Waveform 3	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		Waveform 3	1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	10.0 10.0		ns

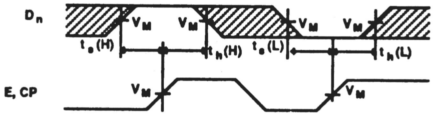
AC WAVEFORMS


1/f MAX
E, CP
V_M
t_w(L)
t_w(H)
t_PHL
t_PLH
Q_n
V_M

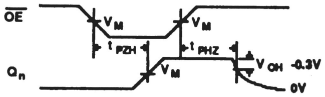
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable and Clock Pulse Widths, and Maximum Clock Frequency


D_n
V_M
t_PLH
t_PHL
Q_n
V_M

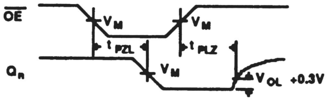
Waveform 2. Propagation Delay For Data To Outputs


D_n
V_M
t_s(H)
t_h(H)
t_s(L)
t_h(L)
E, CP
V_M

Waveform 3. Data Setup And Hold Times


OE
V_M
t_PZH
t_PHZ
Q_n
V_OH -0.3V
0V

Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

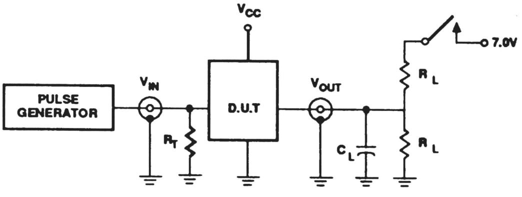

OE
V_M
t_PZL
t_PLZ
Q_n
V_OL +0.3V

Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.3V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
7.0V
R_L
PULSE GENERATOR
V_IN
D.U.T
V_OUT
R_T
C_L
R_L

Test Circuit For 3-State Outputs

SWITCH POSITION

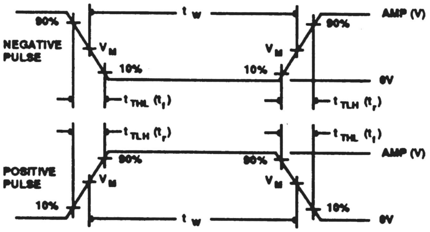
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t_w
AMP (V)
90%
NEGATIVE PULSE
V_M
10%
0V
t_THL (t_f)
t_TLH (t_r)
POSITIVE PULSE
AMP (V)
90%
V_M
10%
0V
t_w

$V_M = 1.3V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS377
Flip-Flop

Octal D Flip-Flop With Enable
Preliminary Specification

FEATURES

- **Ideal for addressable register applications**
- **Enable for address and data synchronization applications**
- **Eight edge-triggered D-type flip-flops**
- **Buffered common clock**
- **See 'ALS273 for Master Reset version**
- **See 'ALS373 for transparent latch version**
- **See 'ALS374 for 3-State version**

DESCRIPTION

The 74ALS377 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS377	50 MHz	15mA

ORDERING INFORMATION

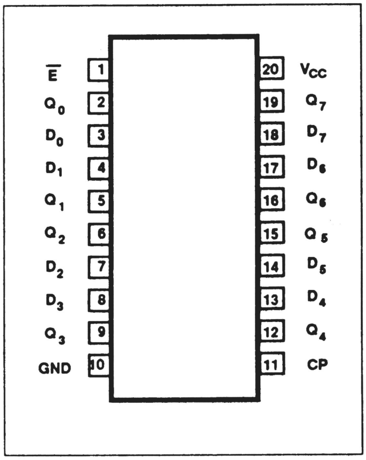
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74ALS377N
20-Pin Plastic SOL	N74ALS377D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

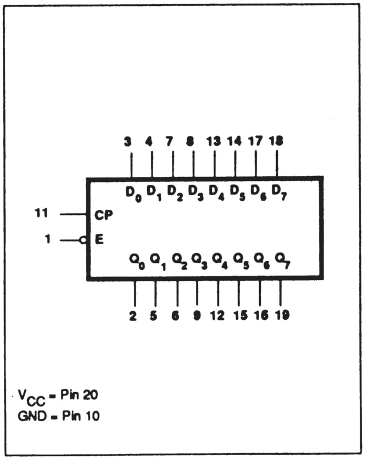
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.1mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.1mA
$\overline{E}$	Enable input (active-Low)	1.0/1.0	20µA/0.1mA
Q_0 - Q_7	Data outputs	130/240	2.6mA/24mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

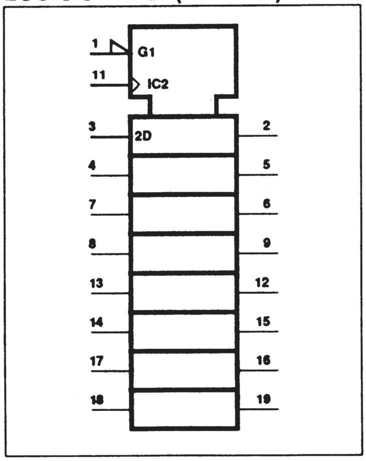
PIN CONFIGURATION


$\overline{E}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 CP

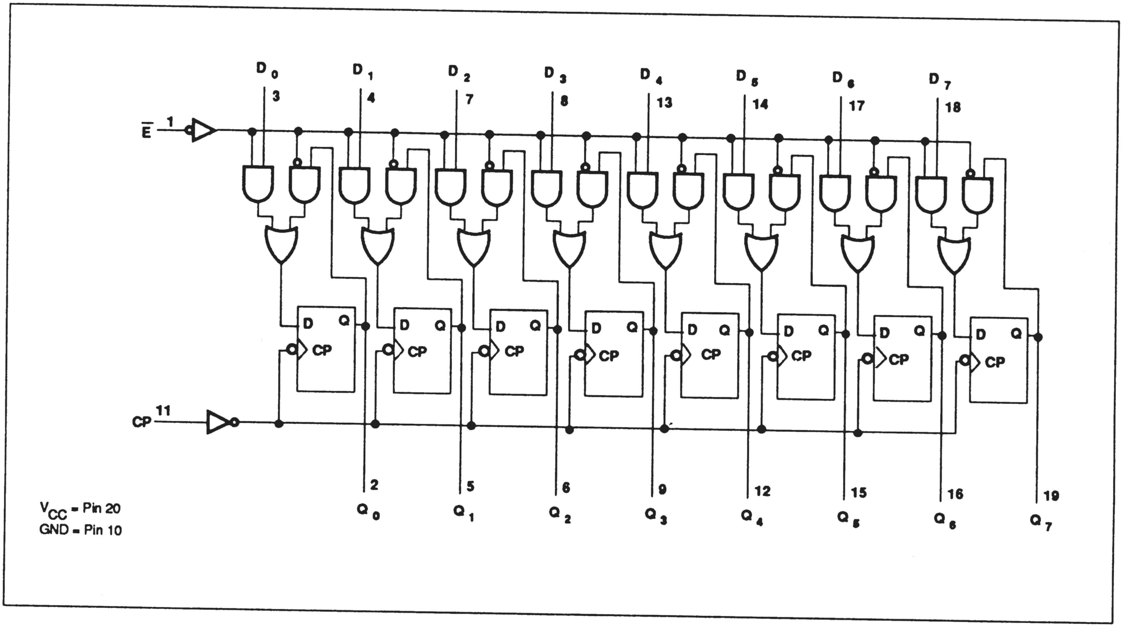
LOGIC SYMBOL


3 4 7 8 13 14 17 18
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 CP
1 E
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
2 5 6 9 12 15 16 19
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)


1
G1
11
IC2
3
2D
2
4
5
7
6
8
9
13
12
14
15
17
16
18
19

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
Ē	CP	D_n	Q_n	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h	↑	X	no change	Hold (do nothing)
H	X	X	no change	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -0.4mA	V_{CC} - 2			V
			V_{CC} = MIN, I_{OH} = -2.6mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 12mA		0.25	0.4	V
			I_{OL} = 24mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$			-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V			20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V			-0.1	mA
I_O[3]	Output current		V_{CC} = MAX, V_O = 2.25V	-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		11	20	mA
		I_{CCL}			19	29	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-ciruit output current, I_{OS}.

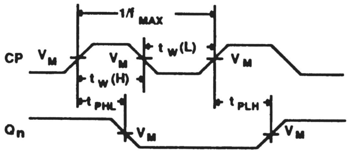
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	35		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n	Waveform 1	2 2	12 15	ns

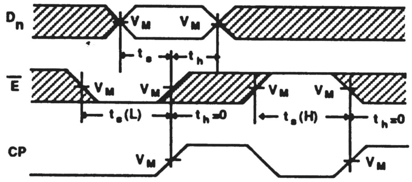
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	10 10		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	15 15		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	14 14		ns

AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency

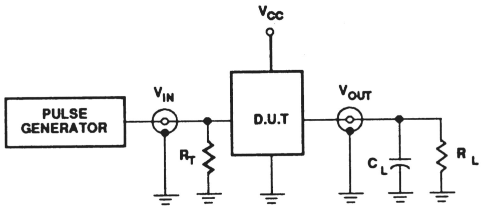


Waveform 2. Data And Enable Setup And Hold Times

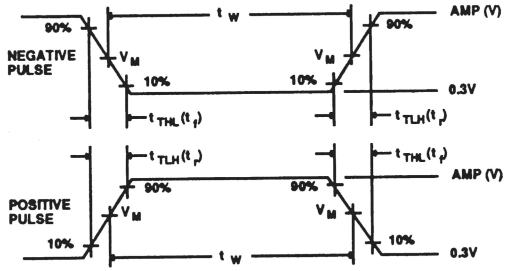
NOTE: For all waveforms, V_M = 1.3V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V$_{CC}$
PULSE GENERATOR
V$_{IN}$
R$_T$
D.U.T
V$_{OUT}$
C$_L$
R$_L$

Test Circuit For Totem-Pole Outputs


t$_W$
AMP (V)
90%
NEGATIVE PULSE
V$_M$
10%
0.3V
t$_{THL}$ (t$_f$)
t$_{TLH}$ (t$_r$)
POSITIVE PULSE
90%
V$_M$
10%
t$_{TLH}$ (t$_r$)
t$_{THL}$ (t$_f$)
AMP (V)
0.3V
t$_W$

$V_M = 1.3V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS543, 74ALS543-1, 74ALS544, 74ALS544-1 Transceivers

74ALS543/'ALS543-1 Octal Registered Transceiver, Non-Inverting (3-State)
74ALS544/ALS544-1 Octal Registered Transceiver, Inverting (3-State)
Preliminary Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS543/74ALS543-1	8.0ns	40mA
74ALS544/74ALS544-1	8.5ns	45mA

FEATURES

- **Combines '245 and '373 type functions in one chip**
- **8-bit octal transceiver with D-type latch**
- **Back-to-back registers for storage**
- **Separate controls for data flow in each direction**
- **The -1 versions sink 48mA I_{OL} within the ± 5%V_{CC} range**
- **300 mil wide 24-pin Slim DIP package**
- **3-state outputs for bus-orientated applications**

DESCRIPTION

The 74ALS543/74ALS543-1 and 74ALS544/74ALS544-1 Octal Registered Transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. While the 'ALS543/'ALS543-1 has non-inverting data path, the 'ALS544/'ALS544-1 inverts data in both directions. The 'ALS543-1 and 'ALS544-1 will sink 48mA if the V_{CC} is limited to 5.0V±0.25V.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	74ALS543N, 74ALS543N-1, 74ALS544N, 74ALS544-1N
24-Pin Plastic SOL	74ALS543D, 74ALS543D-1, 74ALS544D, 74ALS544-1D

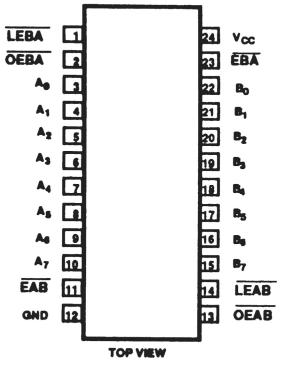
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'543/ '543-1 '544/ '544-1	A_0- A_7	Port A inputs	1.0/1.0	20µA/0.1mA
	B_0- B_7	Port B inputs	1.0/1.0	20µA/0.1mA
	$\overline{OEAB}$	A-to-B Output Enable input (Active Low)	1.0/1.0	20µA/0.1mA
	$\overline{OEBA}$	B-to-A Output Enable input (Active Low)	1.0/1.0	20µA/0.1mA
	$\overline{EAB}$	A-to-B Enable input (Active Low)	1.0/1.0	20µA/0.1mA
	$\overline{EBA}$	B-to-A Enable input (Active Low)	1.0/1.0	20µA/0.1mA
	$\overline{LEAB}$	A-to-B Latch Enable input (Active Low)	1.0/1.0	20µA/0.1mA
	$\overline{LEBA}$	B-to-A Latch Enable input (Active Low)	1.0/1.0	20µA/0.1mA
'543/ '543-1	A_n, B_n	Outputs (All versions)	750/240	15mA/24mA
		Outputs (-1 version)	750/480	15mA/48mA
'544/ '544-1	$\overline{A}_n$, $\overline{B}_n$	Outputs (All versions)	750/240	15mA/24mA
		Outputs (-1 version)	750/480	15mA/48mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

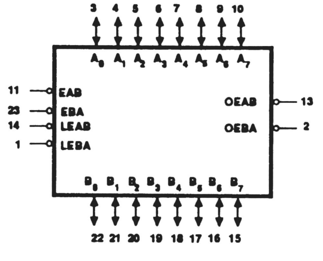
PIN CONFIGURATION

'ALS543/'ALS543-1


LEBA 1
OEBA 2
A0 3
A1 4
A2 5
A3 6
A4 7
A5 8
A6 9
A7 10
EAB 11
GND 12
24 VCC
23 EBA
22 B0
21 B1
20 B2
19 B3
18 B4
17 B5
16 B6
15 B7
14 LEAB
13 OEAB
TOP VIEW

LOGIC SYMBOL

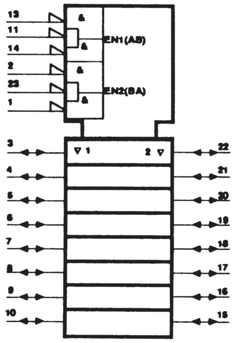
'ALS543/'ALS543-1


3 4 5 6 7 8 9 10
A0 A1 A2 A3 A4 A5 A6 A7
11 EAB
23 EBA
14 LEAB
1 LEBA
OEAB 13
OEBA 2
B0 B1 B2 B3 B4 B5 B6 B7
22 21 20 19 18 17 16 15

V_{CC} = Pin 24
GND = Pin 12

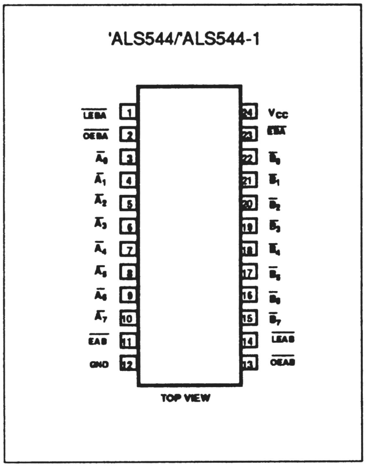
LOGIC SYMBOL(IEEE/IEC)

'ALS543/'ALS543-1

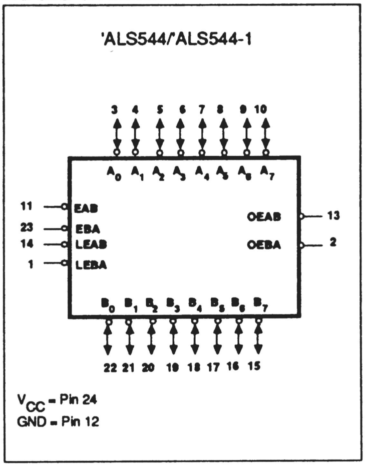

13
11
14
2
23
1
&
EN1(AB)
EN2(BA)
▽1
2▽
3 4 5 6 7 8 9 10
22 21 20 19 18 17 16 15

October 24, 1988

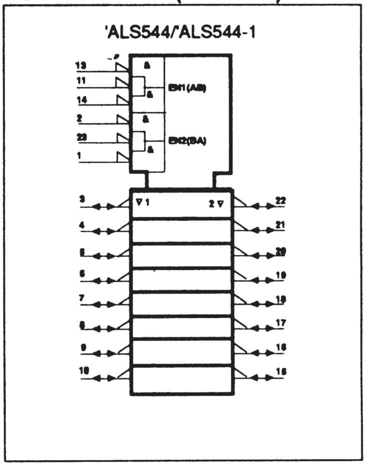
PIN CONFIGURATION


'ALS544/'ALS544-1
LEBA 1
OEBA 2
A0 3
A1 4
A2 5
A3 6
A4 7
A5 8
A6 9
A7 10
EAB 11
GND 12
24 Vcc
23 EBA
22 B0
21 B1
20 B2
19 B3
18 B4
17 B5
16 B6
15 B7
14 LEAB
13 OEAB
TOP VIEW

LOGIC SYMBOL


'ALS544/'ALS544-1
3 4 5 6 7 8 9 10
A0 A1 A2 A3 A4 A5 A6 A7
11 EAB
23 EBA
14 LEAB
1 LEBA
OEAB 13
OEBA 2
B0 B1 B2 B3 B4 B5 B6 B7
22 21 20 19 18 17 16 15
VCC = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)


'ALS544/'ALS544-1
13
11
14
2
23
1
&
EN1(AB)
EN2(BA)
▽1
2▽
3 4 5 6 7 8 9 10
22 21 20 19 18 17 16 15

FUNCTIONAL DESCRIPTION

The 'ALS543/'ALS543-1 and 'ALS544/'ALS544-1 contain two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) input must be Low in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the Function Table. With $\overline{EAB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent Low-to High transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

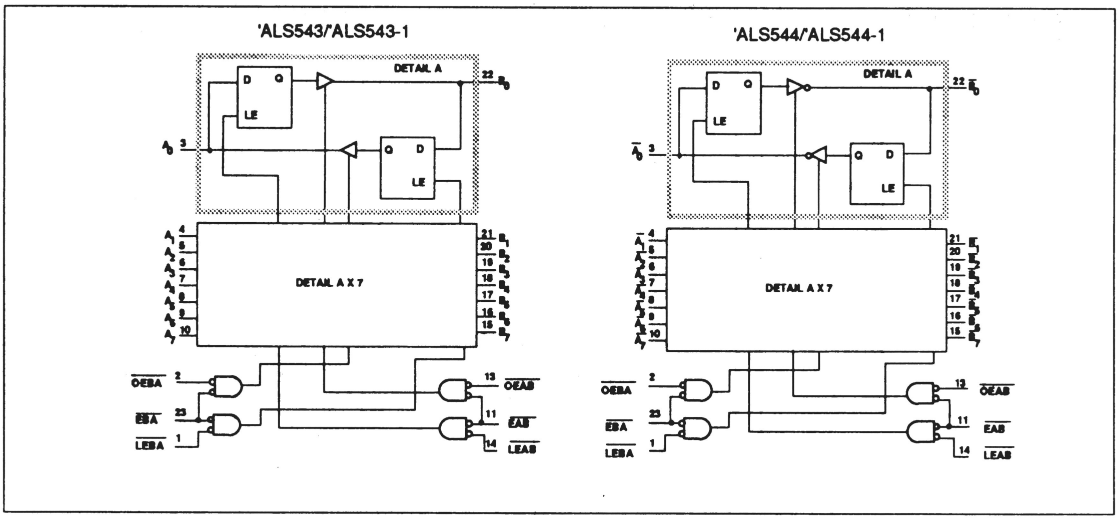
Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

FUNCTION TABLE for 'ALS543/'ALS543-1 and 'ALS544/'ALS544-1

INPUTS				OUTPUTS		STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	DATA	'543/'543-1	'544/'544-1	
H	X	X	X	Z	Z	Disabled
X	H	X	X	Z	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	L H	Latch + Display
L L	L L	L L	H L	H L	L H	Trasparent
L	L	H	X	NC	NC	Hold

H= High voltage level
L= Low voltage level
h= High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to -High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ =Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
X=Don't care
NC=No change
Z =High impedance "off" state

LOGIC DIAGRAM


'ALS543/'ALS543-1
'ALS544/'ALS544-1
DETAIL A
D Q
LE
Q D
LE
DETAIL A X 7
A0
B0
A1
A2
A3
A4
A5
A6
A7
B1
B2
B3
B4
B5
B6
B7
OEBA
EBA
LEBA
OEAB
EAB
LEAB

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 versions	96	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 versions			48[1]	mA
T_A	Operating free-air temperature range		0		70	°C

NOTE 1. The 48mA limit applies only under the condition of V_{CC}=5.0V ± 5%.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} ± 10%	V_{IL} = MAX V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} -2			V
				V_{CC} = MIN		I_{OH} = -3mA	2.4	3.2		V
						I_{OH} = -15mA	2.0			V
V_{OL}	Low-level output voltage	All versions		V_{CC} = MIN	V_{IL} = MAX V_{IH} = MIN	I_{OL} = 12mA		0.25	0.4	V
						I_{OL} = 24mA		0.35	0.5	V
		-1 versions		V_{CC} = 4.75V		I_{OL} = 48mA		0.35	0.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	Control inputs		V_{CC} = MAX, V_I = 7.0V					0.1	mA
		A or B ports		V_{CC} = MAX, V_I = 5.5V					0.1	mA
I_{IH}	High-level input current[3]			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current[3]			V_{CC} = MAX, V_I = 0.4V					-0.2	mA
I_O	Short-circuit output current[4]			V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	'ALS543/ 'ALS543-1	I_{CCH}	V_{CC} = MAX				47	76	mA
			I_{CCL}					55	88	mA
			I_{CCZ}					55	88	mA
		'ALS544/ 'ALS544-1	I_{CCH}					47	76	mA
			I_{CCL}					57	88	mA
			I_{CCZ}					57	88	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS for 'ALS543/'ALS543-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Max	
t_{PLH}	Propagation delay A_n to B_n	Waveform 2	3	15	ns
t_{PHL}			3	15	
t_{PLH}	Propagation delay B_n to A_n	Waveform 2	3	12	ns
t_{PHL}			3	12	
t_{PLH}	Propagation delay $\overline{\text{LEBA}}$ to A_n	Waveform 1, 2	4	11	ns
t_{PHL}			4	11	
t_{PLH}	Propagation delay $\overline{\text{LEAB}}$ to B_n	Waveform 1, 2	4	11	ns
t_{PHL}			4	11	
t_{PZH}	Output Enable time $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to A_n or B_n	Waveform 4	2	15	ns
t_{PZL}		Waveform 5	2	15	
t_{PHZ}	Output Disable time $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to A_n or B_n	Waveform 4	2	15	ns
t_{PLZ}		Waveform 5	2	15	
t_{PZH}	Output Enable time $\overline{\text{EBA}}$ or $\overline{\text{EAB}}$ to A_n or B_n	Waveform 4	2	15	ns
t_{PZL}		Waveform 5	2	15	
t_{PHZ}	Output Disable time $\overline{\text{EBA}}$ or $\overline{\text{EAB}}$ to A_n or B_n	Waveform 4	2	15	ns
t_{PLZ}		Waveform 5	2	15	

AC SETUP REQUIREMENTS for 'ALS543/'ALS543-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Max	
t_s(H)	Setup time, High or Low A_n or B_n to $\overline{\text{LEAB}}$, $\overline{\text{LEBA}}$, $\overline{\text{EAB}}$, or $\overline{\text{EBA}}$	Waveform 3	10		ns
t_s(L)			10		
t_h(H)	Hold time, High or Low A_n or B_n to $\overline{\text{LEAB}}$, $\overline{\text{LEBA}}$, $\overline{\text{EAB}}$, or $\overline{\text{EBA}}$	Waveform 3	0		ns
t_h(L)			0		
t_w(L)	Latch enable Pulse width, Low	Waveform 3	10		ns

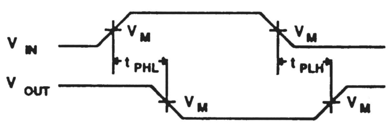
AC ELECTRICAL CHARACTERISTICS for 'ALS544/'ALS544-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$	Waveform 1	3 3	15 15	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{A}_n$	Waveform 1	3 3	12 12	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to $\overline{A}_n$	Waveform 1, 2	4 4	11 11	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to $\overline{B}_n$	Waveform 1, 2	4 4	11 11	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	2 2	15 15	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	2 2	15 15	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ or $\overline{EAB}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	2 2	15 15	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ or $\overline{EAB}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	2 2	15 15	ns

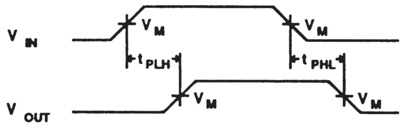
AC SETUP REQUIREMENTS for 'ALS544/'ALS544-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$, or $\overline{EBA}$	Waveform 3	10 10		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$, or $\overline{EBA}$	Waveform 3	0 0		ns
$t_w(L)$	Latch enable Pulse width, Low	Waveform 3	10		ns

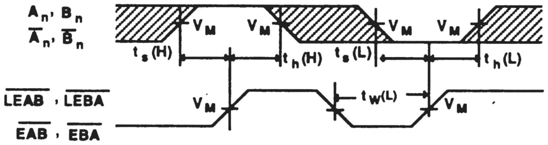
AC WAVEFORMS


V IN
V OUT
V M
t PHL
t PLH

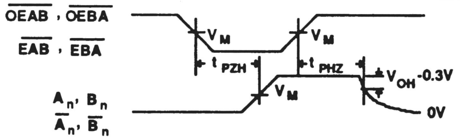
Waveform 1. Propagation Delay For Inverting Output


V IN
V OUT
V M
t PLH
t PHL

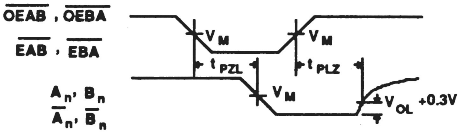
Waveform 2. Propagation Delay For Non-Inverting Output


An, Bn
An, Bn
LEAB, LEBA
EAB, EBA
V M
ts (H)
th (H)
ts (L)
th (L)
tw(L)

Waveform 3. Data Setup And Hold Times And Latch Enable pulse width


OEAB, OEBA
EAB, EBA
An, Bn
An, Bn
V M
t PZH
t PHZ
V OH -0.3V
0V

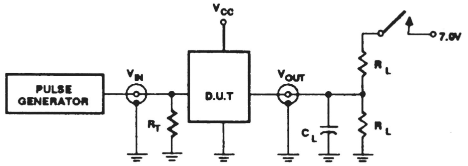
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level


OEAB, OEBA
EAB, EBA
An, Bn
An, Bn
V M
t PZL
t PLZ
V OL +0.3V

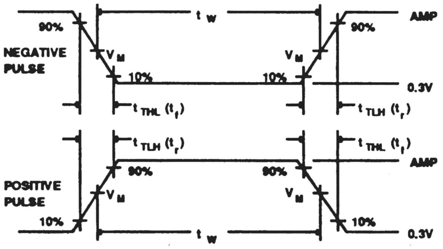
Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.3V$.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS


Vcc
7.0V
PULSE GENERATOR
VIN
D.U.T
VOUT
RL
RT
CL
RL

Test Circuit For 3-State Outputs


90%
NEGATIVE PULSE
VM
10%
tw
AMP
0.3V
tTHL (tf)
tTLH (tr)
POSITIVE PULSE
90%
10%
AMP
0.3V

$V_M = 1.3V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS563A, 74ALS564A

Latch/Flip-Flops

74ALS563A Octal Transparent Latch, Inverting (3-State)
74ALS564A Octal D Flip-Flop, Inverting (3-State)

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS563A	6.0ns	12mA
74ALS564A	6.0ns	15mA

FEATURES

- **74ALS563A is broadside pinout and inverting version of 74ALS373**
- **74ALS564A is broadside pinout and inverting version of 74ALS374**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus Interfacing**
- **Common Output Enable**
- **74ALS573B and 74ALS574A are non-inverting versions of 74ALS563A and 74ALS564A respectively**

DESCRIPTION

The 74ALS563A is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates. The 74ALS563A is a complementary version of the 74ALS373 and has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

ORDERING INFORMATION

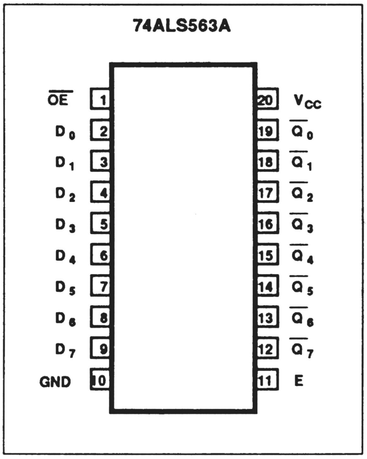
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74ALS563AN, 74ALS564AN
20-Pin Plastic SOL	74ALS563AD, 74ALS564AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

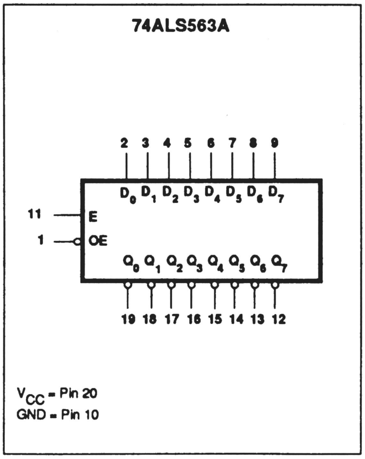
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/2.0	20µA/0.2mA
E ('ALS563A)	Latch enable input	1.0/1.0	20 A/0.1mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.1mA
CP ('ALS564A)	Clock Pulse input (Active rising edge)	1.0/2.0	20 A/0.2mA
$\overline{Q}_0$ - $\overline{Q}_7$	Data outputs	130/240	2.6mA/24mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

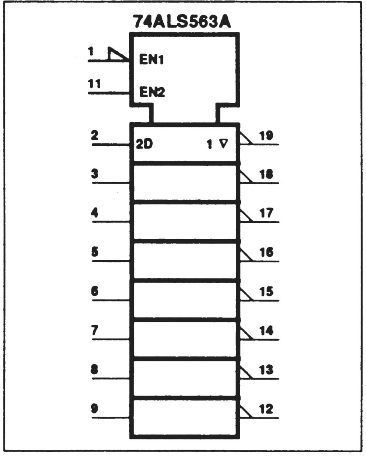

74ALS563A
$\overline{OE}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
GND 10
20 V_{CC}
19 $\overline{Q}_0$
18 $\overline{Q}_1$
17 $\overline{Q}_2$
16 $\overline{Q}_3$
15 $\overline{Q}_4$
14 $\overline{Q}_5$
13 $\overline{Q}_6$
12 $\overline{Q}_7$
11 E

LOGIC SYMBOL

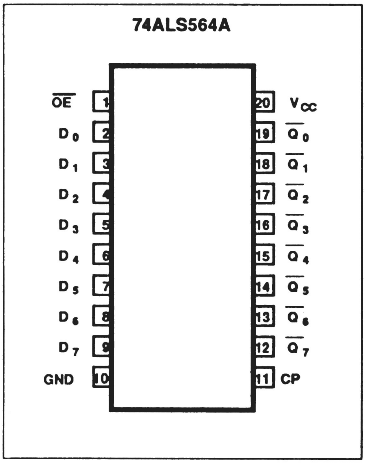

74ALS563A
2 3 4 5 6 7 8 9
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 E
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
19 18 17 16 15 14 13 12

V_{CC} = Pin 20
GND = Pin 10

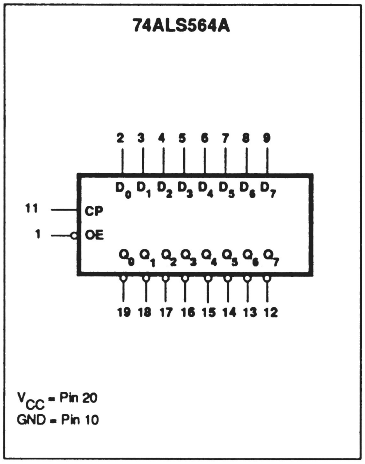
LOGIC SYMBOL(IEEE/IEC)


74ALS563A
1 EN1
11 EN2
2 2D 1 ▽ 19
3 18
4 17
5 16
6 15
7 14
8 13
9 12

PIN CONFIGURATION

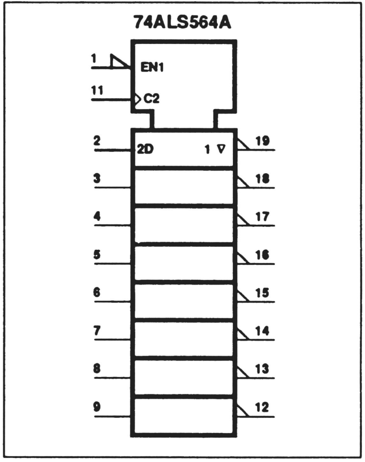

74ALS564A
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 VCC
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 CP

LOGIC SYMBOL


74ALS564A
2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
11 CP
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
19 18 17 16 15 14 13 12

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

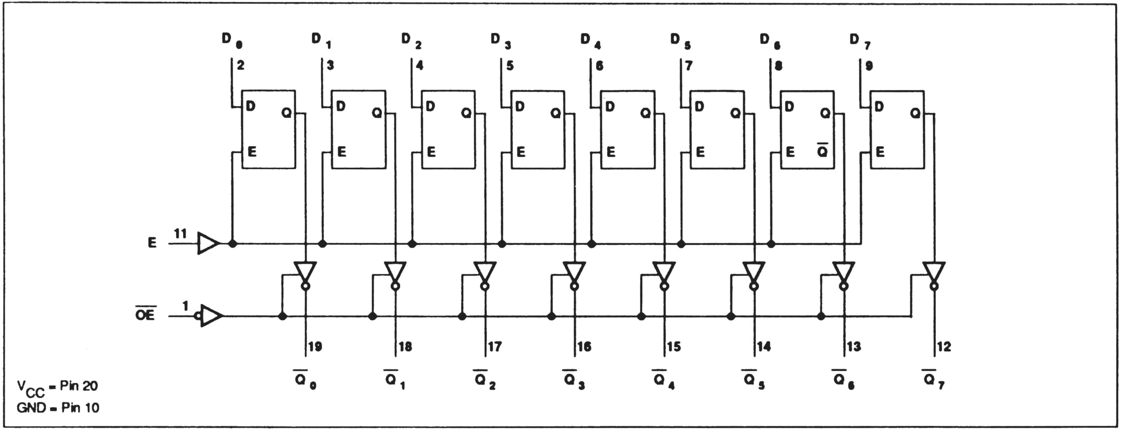

74ALS564A
1 EN1
11 C2
2 2D 1 ▽ 19
3 18
4 17
5 16
6 15
7 14
8 13
9 12

The data on the D inputs is inverted and transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the inverted data that is present one set-up time before the High-to-Low enable transition.

The 74ALS564A is a complementary version of the 74ALS374 and has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors. It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{\text{OE}}$) control gates.
The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is inverted and transferred to the corresponding flip-flop's Q output.

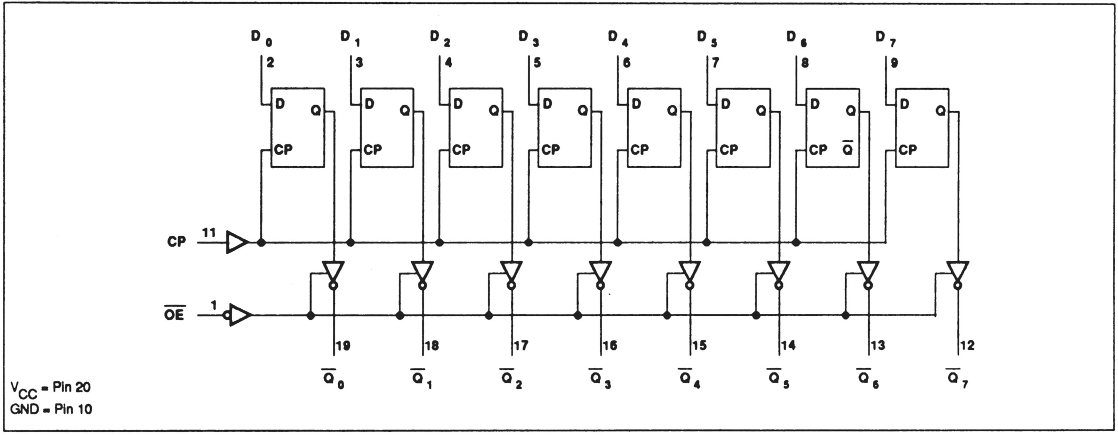
The active Low Output Enable ($\overline{\text{OE}}$) controls all eight 3-State buffers. When $\overline{\text{OE}}$ is Low, the stored or transparent data appears at the outputs. When $\overline{\text{OE}}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 74ALS563A


D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
D Q E
E 11
OE 1
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7

V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 74ALS564A


D0
D1
D2
D3
D4
D5
D6
D7
2
3
4
5
6
7
8
9
D
Q
CP
$\overline{Q}$
CP
11
$\overline{OE}$
1
19
18
17
16
15
14
13
12
$\overline{Q}_0$
$\overline{Q}_1$
$\overline{Q}_2$
$\overline{Q}_3$
$\overline{Q}_4$
$\overline{Q}_5$
$\overline{Q}_6$
$\overline{Q}_7$
V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE, 74ALS563A

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	Q_0 - Q_7	
L L	H H	L H	L H	H L	Enable and read register
L L	↓ ↓	l h	L H	H L	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 74ALS564A

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L L	↑ ↑	l h	L H	H L	Load and read register
L	↑̸	X	NC	NC	Hold
H H	↑ X	D_n X	D_n X	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↑̸ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC}-2			V
				V_{CC}= MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	I_{OL} = 12mA		0.25	0.4	V
				V_{IH} = MIN	I_{OL} = 24mA		0.35	0.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	74ALS563A		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
		74ALS564A						-0.2	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				20	μA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.4V				-20	μA
I_O	Output current[3]			V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	74ALS563A	V_{CC} = MAX			7	12	mA
		I_{CCL}					13	21	mA
		I_{CCZ}					15	24	mA
		I_{CCH}	74ALS564A	V_{CC} = MAX			11	18	mA
		I_{CCL}					17	27	mA
		I_{CCZ}					18	28	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}

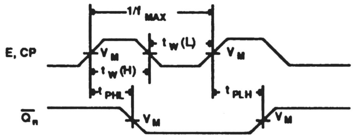
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS		UNIT
				T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74ALS563A	Waveform 2	2.0 3.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$		Waveform 1	4.0 4.0	13.0 13.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	1.0 3.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 2.0	9.0 11.0	ns
f_{MAX}	Maximum Clock frequency	74ALS564A	Waveform 1	50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	3.0 4.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	1.0 3.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 2.0	9.0 11.0	ns

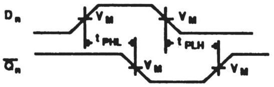
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS		UNIT
				T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	74ALS563A	Waveform 3 Waveform 3	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E		Waveform 3 Waveform 3	6.0 6.0		ns
$t_w(H)$	E Pulse width, High		Waveform 1	10.0		ns
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	74ALS564A	Waveform 3 Waveform 3	6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		Waveform 3 Waveform 3	1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1 Waveform 1	7.0 11.0		ns

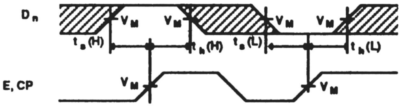
AC WAVEFORMS


1/f MAX
E, CP
V_M
t_W(L)
t_W(H)
t_PHL
t_PLH
Q̄n

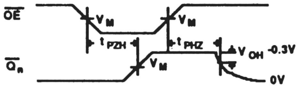
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable and Clock Pulse Widths, and Maximum Clock Frequency


Dn
V_M
t_PHL
t_PLH
Q̄n

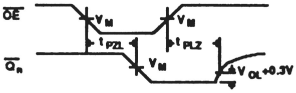
Waveform 2. Propagation Delay For Data To Outputs


Dn
V_M
t_s(H)
t_h(H)
t_s(L)
t_h(L)
E, CP

Waveform 3. Data Setup And Hold Times


OE
V_M
t_PZH
t_PHZ
V_OH -0.3V
Q̄n
0V

Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

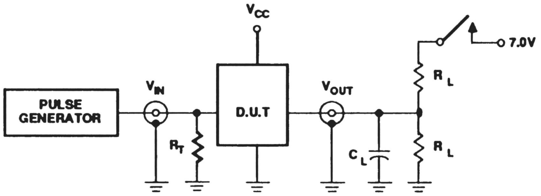

OE
V_M
t_PZL
t_PLZ
V_OL+0.3V
Q̄n

Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

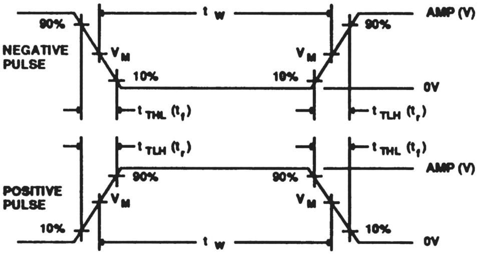
NOTE: For all waveforms, $V_M = 1.3V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
PULSE GENERATOR
V_IN
R_T
D.U.T
V_OUT
C_L
R_L
R_L
7.0V

Test Circuit For 3-State Outputs


t_W
90%
AMP (V)
NEGATIVE PULSE
V_M
10%
0V
t_THL (t_f)
t_TLH (t_r)
POSITIVE PULSE

$V_M = 1.3V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS573B, 74ALS574A
Latch/Flip-Flops

74ALS573B Octal Transparent Latch (3-State)
74ALS574A Octal D Flip-Flop (3-State)
Product Specification

FEATURES

- **74ALS573B is broadside pinout version of 74ALS373**
- **74ALS574A is broadside pinout version of 74ALS374**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus interfacing**
- **Common Output Enable**
- **74ALS563A and 74ALS564A are inverting version of 74ALS573B and 74ALS574A respectively**

DESCRIPTION

The 74ALS573B is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates. The 74ALS573B is functionally identical to the 74ALS373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS573B	5.0ns	12mA
74ALS574A	6.0ns	15mA

ORDERING INFORMATION

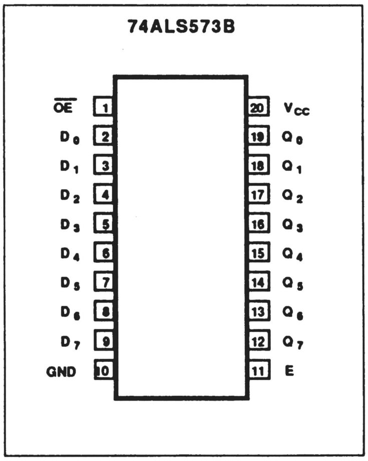
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74ALS573BN, 74ALS574AN
20-Pin Plastic SOL	74ALS573BD, 74ALS574AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/2.0	20μA/0.2mA
E ('ALS573B)	Latch enable input	1.0/1.0	20 A/0.1mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20μA/0.1mA
CP ('ALS574A)	Clock Pulse input (Active rising edge)	1.0/2.0	20 A/0.2mA
Q_0 - Q_7	Data outputs	130/240	2.6mA/24mA

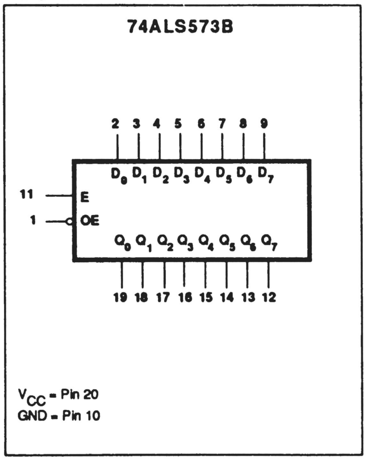
NOTE:
One (1.0) ALS Unit Load is defined as: 20μA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION



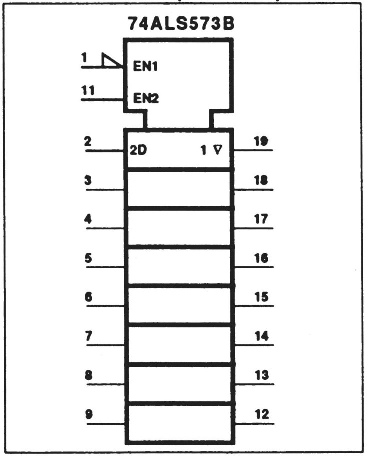
74ALS573B
OE 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 Vcc
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 E

LOGIC SYMBOL



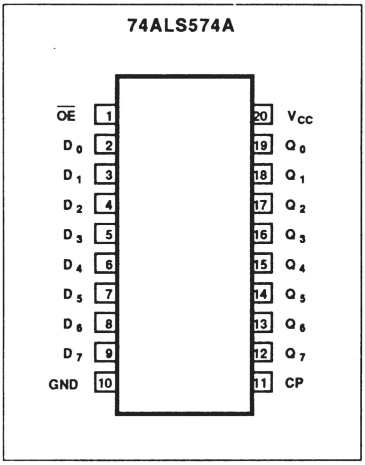
74ALS573B
2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
11 E
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
19 18 17 16 15 14 13 12
VCC = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

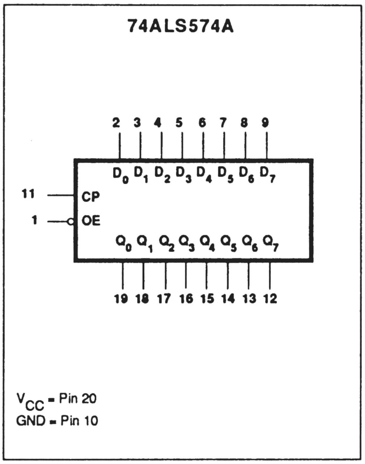


74ALS573B
1 EN1
11 EN2
2 2D 1 ▽ 19
3 18
4 17
5 16
6 15
7 14
8 13
9 12

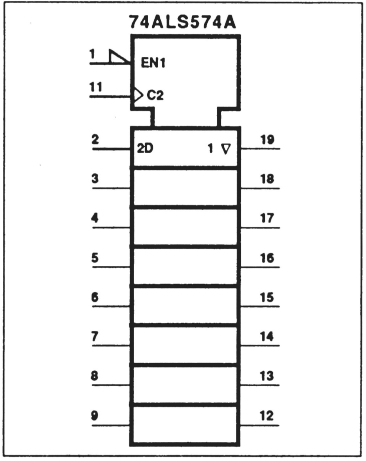
PIN CONFIGURATION


74ALS574A
$\overline{\text{OE}}$ 1
D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
GND 10
20 V_{CC}
19 Q_0
18 Q_1
17 Q_2
16 Q_3
15 Q_4
14 Q_5
13 Q_6
12 Q_7
11 CP

LOGIC SYMBOL


74ALS574A
2 3 4 5 6 7 8 9
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 CP
1 OE
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
19 18 17 16 15 14 13 12
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)


74ALS574A
1
EN1
11
C2
2
2D
1 ∇
19
3
18
4
17
5
16
6
15
7
14
8
13
9
12

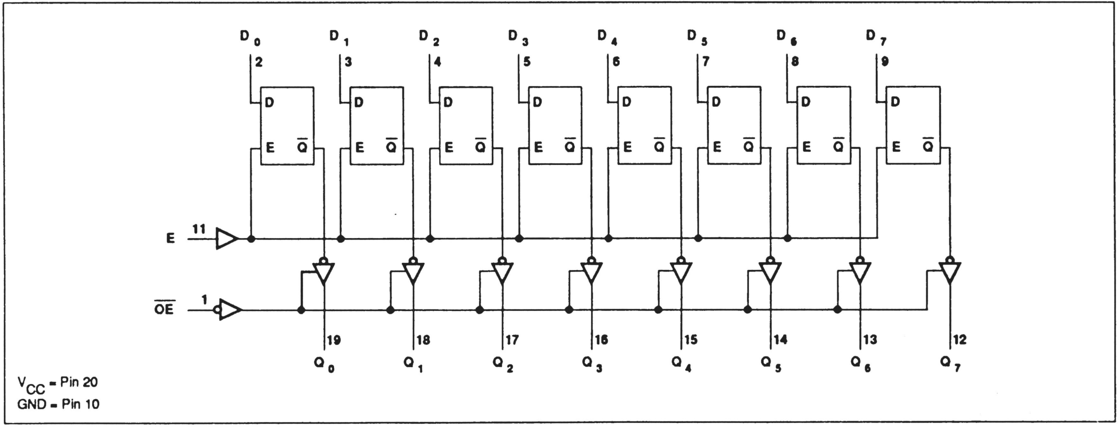
The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

The 74ALS574A is functionally identical to the 74ALS374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors. It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{\text{OE}}$) control gates.

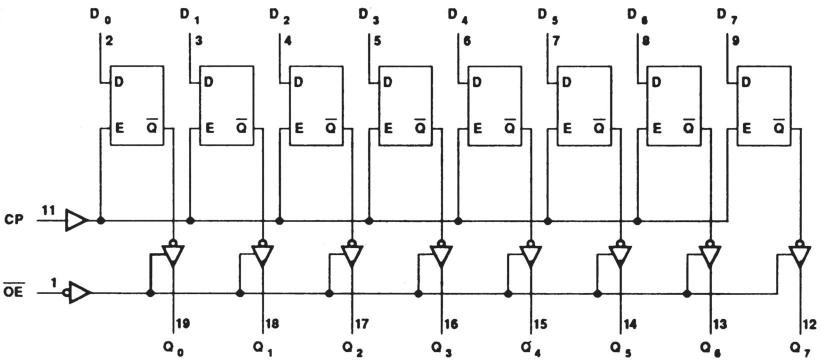
The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The active Low Output Enable ($\overline{\text{OE}}$) controls all eight 3-State buffers. When $\overline{\text{OE}}$ is Low, the stored or transparent data appears at the outputs. When $\overline{\text{OE}}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 74ALS573B


D_0 2
D_1 3
D_2 4
D_3 5
D_4 6
D_5 7
D_6 8
D_7 9
D
E $\overline{Q}$
E 11
$\overline{\text{OE}}$ 1
19 Q_0
18 Q_1
17 Q_2
16 Q_3
15 Q_4
14 Q_5
13 Q_6
12 Q_7
V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 74ALS574A



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE, 74ALS573B

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
OE̅	E	D_n	REGISTER	Q_0 - Q_7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 74ALS574A

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
OE̅	CP	D_n	REGISTER	Q_0 - Q_7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	‡	X	NC	NC	Hold
H H	↑ X	D_n X	D_n X	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC}-2			V
				V_{CC}= MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	I_{OL} = 12mA		0.25	0.4	V
				V_{IH} = MIN	I_{OL} = 24mA		0.35	0.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	74ALS573B		V_{CC} = MAX, V_I = 0.4V				-0.1	mA
		74ALS574A						-0.2	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				20	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.4V				-20	µA
I_O	Output current[3]			V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	74ALS573B	V_{CC} = MAX			7	12	mA
		I_{CCL}					13	21	mA
		I_{CCZ}					15	24	mA
		I_{CCH}	74ALS574A	V_{CC} = MAX			10	16	mA
		I_{CCL}					17	27	mA
		I_{CCZ}					18	28	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}

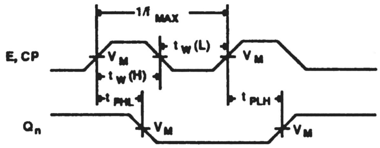
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS		UNIT
				T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74ALS573B	Waveform 2	2.0 2.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 1	4.0 4.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.0 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 2.0	9.0 11.0	ns
f_{MAX}	Maximum Clock frequency	74ALS574A	Waveform 1	45		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	3.0 4.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.0 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 2.0	9.0 11.0	ns

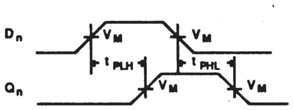
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS		UNIT
				T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Max	
t_s(H) t_s(L)	Set-up time D_n to E	74ALS573B	Waveform 3 Waveform 3	6.0 6.0		ns
t_h(H) t_h(L)	Hold time D_n to E		Waveform 3 Waveform 3	6.0 6.0		ns
t_w(H)	E Pulse width, High		Waveform 1	10.0		ns
t_s(H) t_s(L)	Set-up time D_n to CP	74ALS574A	Waveform 3 Waveform 3	6.0 6.0		ns
t_h(H) t_h(L)	Hold time D_n to CP		Waveform 3 Waveform 3	1.0 1.0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low		Waveform 1 Waveform 1	8.0 12.0		ns

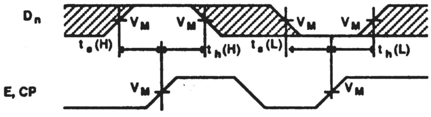
AC WAVEFORMS


E, CP
Qn
1/f MAX
tw(L)
tw(H)
tPHL
tPLH
VM

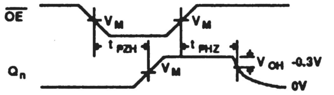
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable and Clock Pulse Widths, and Maximum Clock Frequency


Dn
Qn
VM
tPLH
tPHL

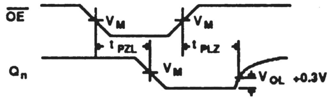
Waveform 2. Propagation Delay For Data To Outputs


Dn
E, CP
VM
ts(H)
th(H)
ts(L)
th(L)

Waveform 3. Data Setup And Hold Times


OE
Qn
VM
tPZH
tPHZ
VOH -0.3V
0V

Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

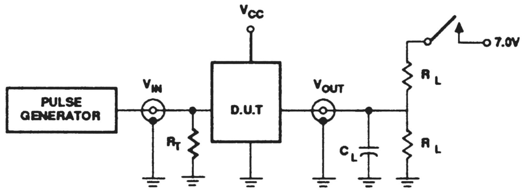

OE
Qn
VM
tPZL
tPLZ
VOL +0.3V

Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

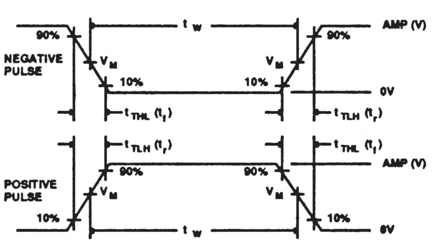
NOTE: For all waveforms, $V_M = 1.3V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


VCC
PULSE GENERATOR
VIN
RT
D.U.T
VOUT
CL
RL
RL
7.0V

Test Circuit For 3-State Outputs


NEGATIVE PULSE
POSITIVE PULSE
90%
10%
VM
tw
tTHL (tf)
tTLH (tr)
AMP (V)
0V

$V_M = 1.3V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS620A, 74ALS620A-1
74ALS623A, 74ALS623A-1
Transceivers

74ALS620A/620A-1 Octal Bus Transceiver, Inverting (3-State)
74ALS623A/623A-1 Octal Bus Transceiver, Non-Inverting (3-State)
Product Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-state buffer outputs sink 24mA and source 15mA**
- **The -1 version sinks 48mA I_{OL} within the ±5% V_{CC} range**

DESCRIPTION

The 74ALS620A and 74ALS623A are octal bus transceivers featuring 3-state bus-compatible outputs in both send and receive directions. The 74ALS620A is an inverting version of the 74ALS623A. The outputs are capable of sinking 24mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The outputs for the 74ALS620A-1 and 74ALS623A-1 are capable of sinking up to 48mA when within the ±5% V_{CC} range. These octal bus transceivers are designed for asynchronous two-way communication between data busses . The control function implementation allows for maximum flexibilty in timing. These devices allow data transmission from the A bus to the B bus or from B bus to A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the busses are effectively isolated. The dual-enable configuration gives the 'ALS620A and 'ALS623A the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS620A/620A-1	4ns	33mA
74ALS623A/623A-1	4ns	38mA

ORDERING INFORMATION

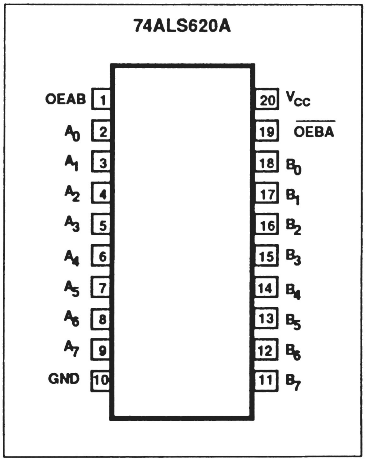
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74ALS620AN, 7AL620A-1N, 74ALS623AN, 7AL623A-1N
20-Pin Plastic SOL	74ALS623AD, 7AL623A-1D, 74ALS623AD, 7AL623A-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

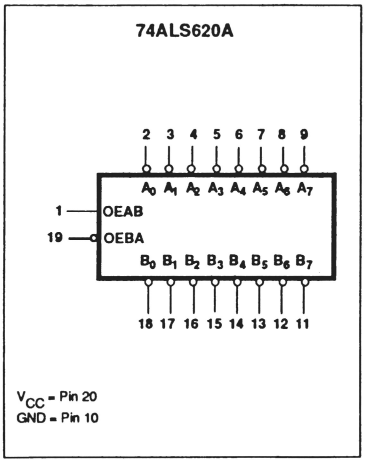
PINS	· DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	1.0/1.0	20μA/20μA
$\overline{OEBA}$, OEAB	Output enable inputs	1.0/1.0	20μA/20μA
A_n, B_n	Data outputs	750/240	15mA/24mA
A_n, B_n	Data outputs (-1 version)	750/480	15mA/48mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20μA in the High state and 0.1mA in the Low state.

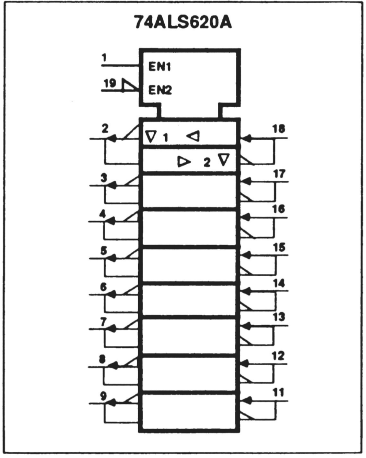
PIN CONFIGURATION


74ALS620A
OEAB 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
GND 10
20 VCC
19 OEBA
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7

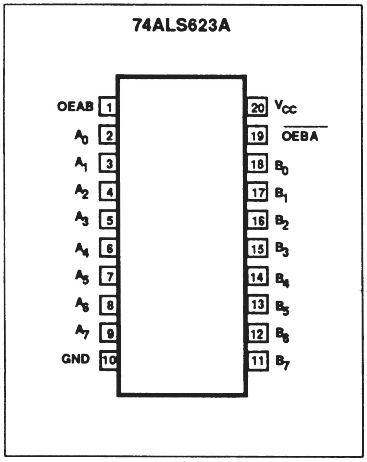
LOGIC SYMBOL


74ALS620A
2 3 4 5 6 7 8 9
A0 A1 A2 A3 A4 A5 A6 A7
1 OEAB
19 OEBA
B0 B1 B2 B3 B4 B5 B6 B7
18 17 16 15 14 13 12 11
VCC = Pin 20
GND = Pin 10

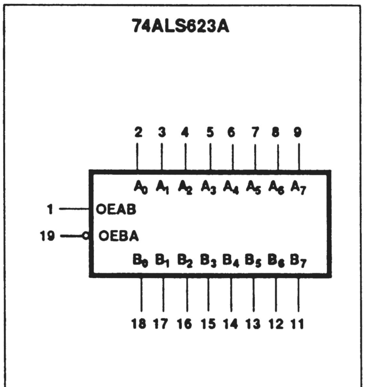
LOGIC SYMBOL(IEEE/IEC)


74ALS620A
1
EN1
19
EN2
▽1 ◁
▷ 2▽
2 3 4 5 6 7 8 9
18 17 16 15 14 13 12 11

PIN CONFIGURATION

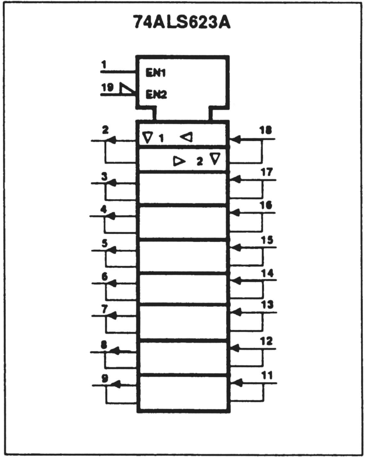

74ALS623A
OEAB 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
GND 10
20 VCC
19 OEBA
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7

LOGIC SYMBOL

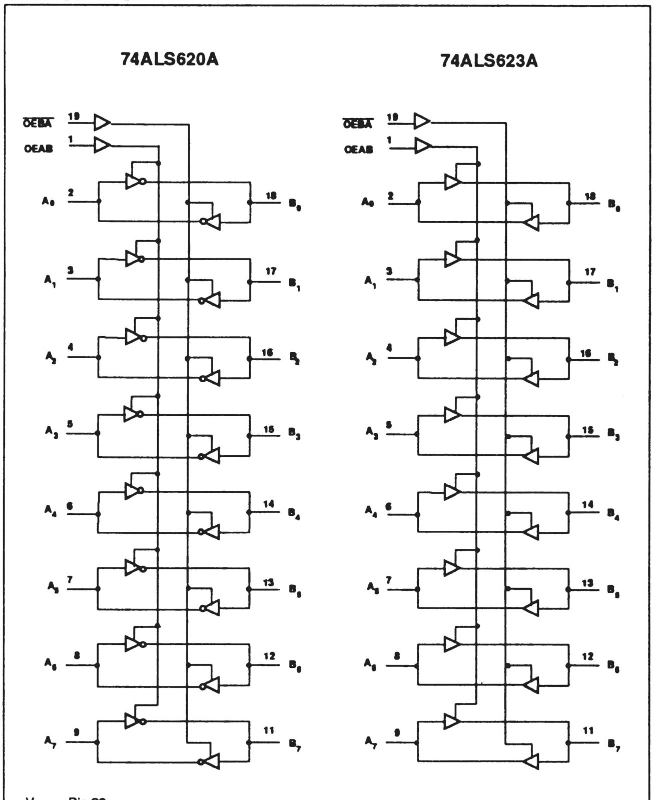

74ALS623A
2 3 4 5 6 7 8 9
A0 A1 A2 A3 A4 A5 A6 A7
1 OEAB
19 OEBA
B0 B1 B2 B3 B4 B5 B6 B7
18 17 16 15 14 13 12 11

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)


74ALS623A
1
19
EN1
EN2
∇1
◁
▷
2∇
2 3 4 5 6 7 8 9
18 17 16 15 14 13 12 11

LOGIC DIAGRAM


74ALS620A
74ALS623A
OEBA 19
OEAB 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7

V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS		OPERATING MODES	
$\overline{\text{OEBA}}$	OEAB	74ALS620A	74ALS623A
L	L	$\overline{\text{B}}$ data to A bus	B data to A bus
H	H	$\overline{\text{A}}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{\text{B}}$ data to A bus $\overline{\text{A}}$ data to B bus	B data to A bus A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version only	96	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version only			48[1]	mA
T_A	Operating free-air temperature range		0		70	°C

NOTE: 1. The 48 mA limit applies only under the condition of V_{CC} = 5.0V±5%.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} ± 10%	V_{IL} = MAX V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} -2			V
				V_{CC} = MIN		I_{OH} = -3mA	2.4	3.2		V
						I_{OH} = -15mA	2.0			V
V_{OL}	Low-level output voltage	All versions		V_{CC} = MIN	V_{IL} = MAX V_{IH} = MIN	I_{OL} = 12mA		0.25	0.4	V
						I_{OL} = 24mA		0.35	0.5	V
		-1 version		V_{CC} = 4.75V		I_{OL} = 48mA		0.35	0.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.5	V
I_I	Input current at maximum input voltage	$\overline{OEBA}$ or OEAB		V_{CC} = MAX, V_I = 7.0V					0.1	mA
		A or B ports		V_{CC} = MAX, V_I = 5.5V					0.1	mA
I_{IH}	High-level input current[3]			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current[3]			V_{CC} = MAX, V_I = 0.4V					-0.1	mA
I_O	Short-circuit output current[4]			V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	74ALS620A 74ALS620A-1	I_{CCH}	V_{CC} = MAX				24	34	mA
			I_{CCL}					42	49	mA
			I_{CCZ}					45	52	mA
		74ALS623A 74ALS623A-1	I_{CCH}	V_{CC} = MAX				29	43	mA
			I_{CCL}					41	50	mA
			I_{CCZ}					46	55	mA

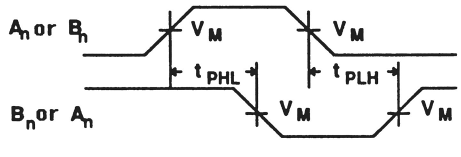
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

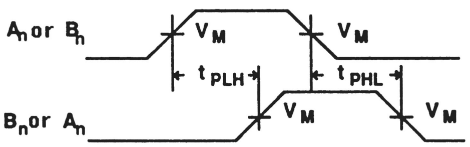
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
				Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	74ALS620A 74ALS620A-1	Waveform 1	2.0 2.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to A_n		Waveform 3 Waveform 4	2.0 3.0	17.0 25.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to A_n		Waveform 3 Waveform 4	2.0 2.0	12.0 18.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB to B_n		Waveform 3 Waveform 4	2.0 3,0	18.0 25.0	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB to B_n		Waveform 3 Waveform 4	2.0 3.0	12.0 18.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	74ALS623A 74ALS623A-1	Waveform 1	2.0 2.0	13.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to A_n		Waveform 3 Waveform 4	2.0 3.0	22.0 22.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to A_n		Waveform 3 Waveform 4	2.0 2.0	16.0 19.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB to B_n		Waveform 3 Waveform 4	2.0 3.0	22.0 22.0	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB to B_n		Waveform 3 Waveform 4	2.0 2.0	16.0 19.0	ns

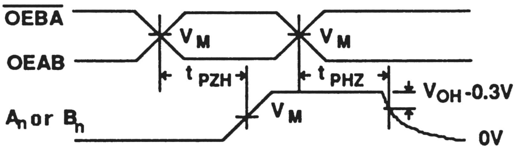
AC WAVEFORMS


A_n or B_n
V_M
V_M
t_{PHL}
t_{PLH}
B_n or A_n
V_M
V_M

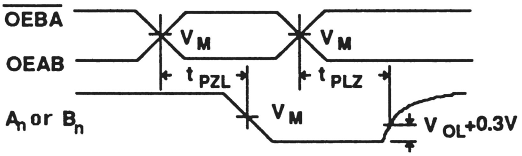
Waveform 1. For Inverting Outputs


A_n or B_n
V_M
V_M
t_{PLH}
t_{PHL}
B_n or A_n
V_M
V_M

Waveform 2. For Non-Inverting Outputs


$\overline{OEBA}$
OEAB
V_M
V_M
t_{PZH}
t_{PHZ}
V_{OH}-0.3V
A_n or B_n
V_M
0V

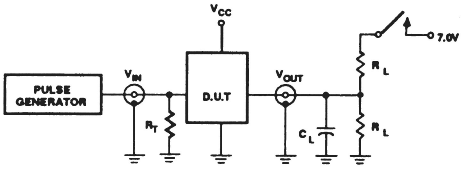
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{OEBA}$
OEAB
V_M
V_M
t_{PZL}
t_{PLZ}
A_n or B_n
V_M
V_{OL}+0.3V

Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.3V.

TEST CIRCUIT AND WAVEFORMS


V_CC
7.0V
R_L
PULSE GENERATOR
V_IN
D.U.T
V_OUT
R_T
C_L
R_L

Test Circuit For 3-State Outputs

SWITCH POSITION

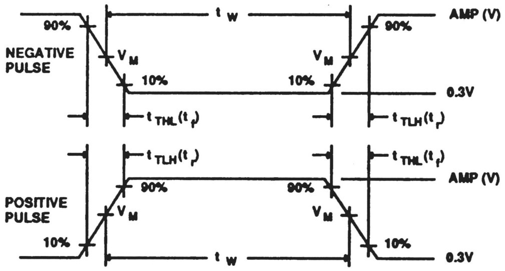
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


t_W
AMP (V)
90%
NEGATIVE PULSE
V_M
10%
0.3V
t_THL(t_f)
t_TLH(t_r)
POSITIVE PULSE
90%
V_M
10%
AMP (V)
0.3V
t_W

$V_M = 1.3V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS645A, 74ALS645A-1
Transceivers

Octal Transceivers (3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS645A 74ALS645A-1	7.0ns	34mA

FEATURES

- **Octal bidirectional bus interface**
- **3-state buffer outputs sink 24mA and source 15mA.**
- **Outputs are placed in high impedance state during power-off conditions**
- **The -1 version sinks 48mA I_{OL} within the ±5% V_{CC} range**

DESCRIPTION

The 74ALS645A is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both transmit and receive directions. The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive(T/$\overline{R}$) input for direction control. The 74ALS645A-1 is the same as the 74ALS645A except that the B port sinks 48 mA within the ±5% V_{CC} range.

ORDERING INFORMATION

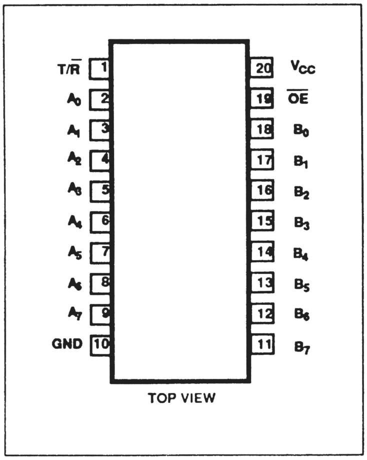
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74ALS645AN, N7AL645A-1N
20-Pin Plastic SOL	N74ALS645AD, N7AL645A-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

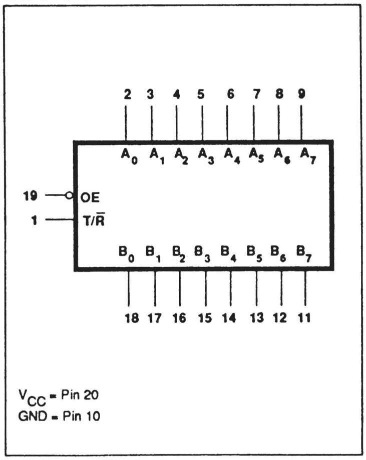
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.1mA
T/$\overline{R}$	Transmit/Receive input	1.0/1.0	20µA/0.1mA
A_0- A_7	A port outputs	750/240	15mA/24mA
B_0- B_7	B Port outputs	750/240	15mA/24mA
B_0- B_7	B Port outputs (-1 version)	750/480	15mA/48mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

PIN CONFIGURATION

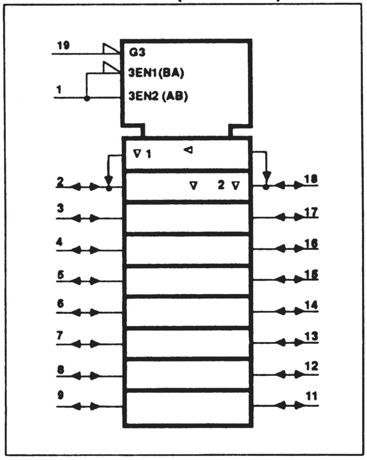

T/R̄ 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
GND 10
20 VCC
19 OE̅
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
TOP VIEW

LOGIC SYMBOL


2 3 4 5 6 7 8 9
A0 A1 A2 A3 A4 A5 A6 A7
19 OE
1 T/R̄
B0 B1 B2 B3 B4 B5 B6 B7
18 17 16 15 14 13 12 11

V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

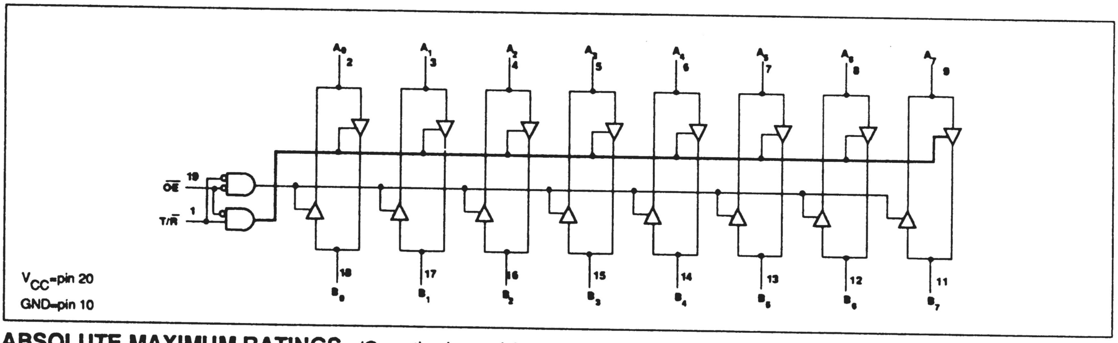

19
1
G3
3EN1(BA)
3EN2 (AB)
∇ 1
◁
∇ 2 ∇
2 3 4 5 6 7 8 9
18 17 16 15 14 13 12 11

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version only	96	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version only			48[1]	mA
T_A	Operating free-air temperature range		0		70	°C

NOTE: 1. The 48 mA limit applies only under the condition of V_{CC} = 5.0V±5%.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} ± 10%	V_{IL} = MAX V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} -2			V
			V_{CC} = MIN		I_{OH} = -3mA	2.4	3.2		V
					I_{OH} = -15mA	2.0			V
V_{OL}	Low-level output voltage	All versions	V_{CC} = MIN	V_{IL} = MAX V_{IH} = MIN	I_{OL} = 12mA		0.25	0.4	V
					I_{OL} = 24mA		0.35	0.5	V
		-1 version	V_{CC} = 4.75V		I_{OL} = 48mA		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.5	V
I_I	Input current at maximum input voltage - $\overline{OE}$ or $T/\overline{R}$		V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_I	Input current at maximum input voltage - A or B ports		V_{CC} = MAX, V_I = 5.5V					0.1	mA
I_{IH}	High-level input current[3]		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current[3]		V_{CC} = MAX, V_I = 0.4V					-0.1	mA
I_O	Short-circuit output current[4]		V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				28	45	mA
		I_{CCL}					40	55	mA
		I_{CCZ}					44	58	mA

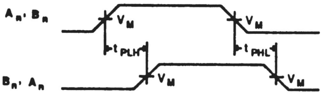
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

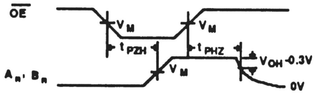
SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2 2	10 10	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	3 3	20 20	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	2 4	10 15	ns

AC WAVEFORMS



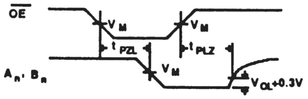
A_n, B_n
V_M
t_{PLH}
t_{PHL}
B_n, A_n

Waveform 1. Propagation Delay For Non-Inverting Output



$\overline{OE}$
V_M
t_{PZH}
t_{PHZ}
V_{OH}-0.3V
0V
A_n, B_n

Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level

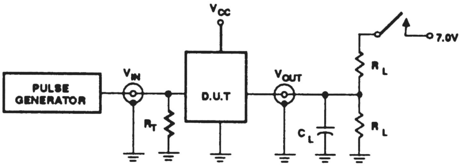


$\overline{OE}$
V_M
t_{PZL}
t_{PLZ}
V_{OL}+0.3V
A_n, B_n

Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

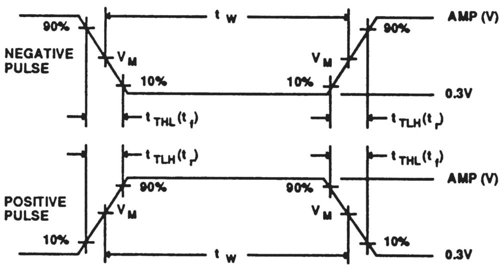
NOTE: For all waveforms, V_M = 1.3V.

TEST CIRCUIT AND WAVEFORMS



V_{CC}
PULSE GENERATOR
V_{IN}
D.U.T
V_{OUT}
7.0V
R_L
R_T
C_L
R_L

Test Circuit For 3-State Outputs



t_W
AMP (V)
90%
NEGATIVE PULSE
V_M
10%
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
POSITIVE PULSE

V_M = 1.3V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS646, 74ALS646-1
74ALS648, 74ALS648-1
Transceivers/Registers

'ALS646/646-1 Octal Transceiver/Register, Non-Inverting (3-state)
'ALS648/648-1 Octal Transceiver/Register, Inverting (3-state)
Preliminary Specification

FEATURES

- **Combines '245 and '374 type functions in one chip**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-state outputs**
- **The -1 version sinks 48mA I_{OL} within the ±5% V_{CC} range**

DESCRIPTION

The 74ALS646/74ALS646-1 and 74ALS648/74ALS648-1 Transceivers/Registers consist of bus transceiver circuits with 3-state outputs , D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$), direction (DIR) and Select (SAB, SBA) pins are provided for bus management. The 74ALS646-1 and 74ALS648-1 will sink 48mA if the V_{CC} is limited to 5.0V±0.25V.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS646/646-1	50MHz	50mA
74ALS648/648-1	50MHz	54mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Dip (300 mil)	74ALS646N, 74ALS646-1N, 74ALS648N, 74ALS648-1N
24-Pin Plastic SOL	74ALS646D, 74ALS646-1D, 74ALS648D, 74ALS648-1D

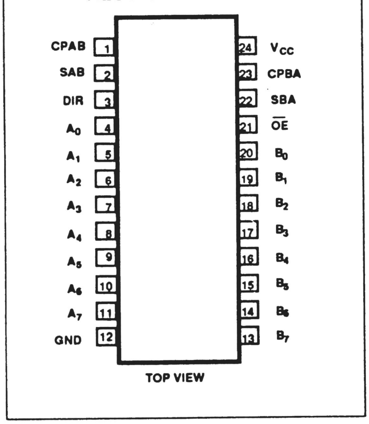
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	1.0/2.0	20µA/0.2mA
B_0 - B_7	B inputs	1.0/2.0	20µA/0.2mA
CPAB	A-to-B clock input	1.0/2.0	20µA/0.2mA
CPBA	B-to-A clock input	1.0/2.0	20µA/0.2mA
SAB	A-to-B select input	1.0/2.0	20µA/0.2mA
SBA	B-to-A select input	1.0/2.0	20µA/0.2mA
DIR	Data flow directional control input	1.0/2.0	20µA/0.2mA
$\overline{OE}$	Output enable input	1.0/2.0	20µA/0.2mA
A_n, B_n	Outputs	750/240	15mA/24mA
A_n, B_n	Outputs (-1 version)	750/480	15mA/48mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

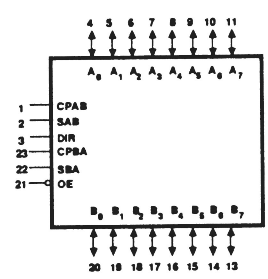
PIN CONFIGURATION

'ALS646/'ALS646-1


CPAB 1
SAB 2
DIR 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
GND 12
24 VCC
23 CPBA
22 SBA
21 OE
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
TOP VIEW

LOGIC SYMBOL

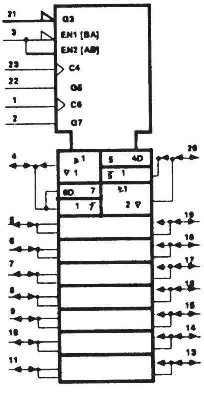
'ALS646/'ALS646-1


4 5 6 7 8 9 10 11
A0 A1 A2 A3 A4 A5 A6 A7
1 CPAB
2 SAB
3 DIR
23 CPBA
22 SBA
21 OE
B0 B1 B2 B3 B4 B5 B6 B7
20 19 18 17 16 15 14 13

V_{CC} = Pin 24
GND = Pin 12

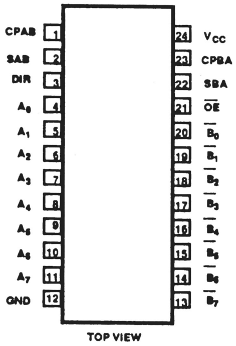
LOGIC SYMBOL(IEEE/IEC)

'ALS646/'ALS646-1


21
3
23
22
1
2
G3
EN1 [BA]
EN2 [AB]
C4
G5
C6
G7
4
20
5
6
7
8
9
10
11
19
18
17
16
15
14
13

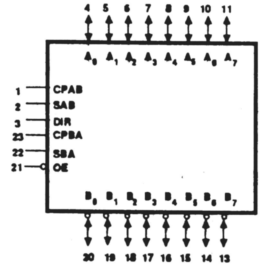
PIN CONFIGURATION

'ALS648/'ALS648-1


CPAB
1
SAB
2
DIR
3
A_0
4
A_1
5
A_2
6
A_3
7
A_4
8
A_5
9
A_6
10
A_7
11
GND
12
24
V_{CC}
23
CPBA
22
SBA
21
$\overline{OE}$
20
$\overline{B_0}$
19
$\overline{B_1}$
18
$\overline{B_2}$
17
$\overline{B_3}$
16
$\overline{B_4}$
15
$\overline{B_5}$
14
$\overline{B_6}$
13
$\overline{B_7}$
TOP VIEW

LOGIC SYMBOL

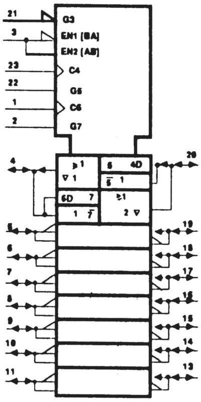
'ALS648/'ALS648-1


4 5 6 7 8 9 10 11
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
1 CPAB
2 SAB
3 DIR
23 CPBA
22 SBA
21 OE
$\overline{B_0}$ $\overline{B_1}$ $\overline{B_2}$ $\overline{B_3}$ $\overline{B_4}$ $\overline{B_5}$ $\overline{B_6}$ $\overline{B_7}$
20 19 18 17 16 15 14 13

V_{CC} = Pin 24
GND = Pin 12

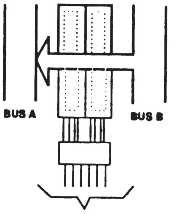
LOGIC SYMBOL(IEEE/IEC)

'ALS648/'ALS648-1


21
3
23
22
1
2
G3
EN1 (BA)
EN2 (AB)
C4
G5
C6
G7
4
≥1
▽ 1
5 4D
$\overline{5}$ 1
6D 7
1 $\overline{7}$
≥1
2 ▽
20
5
6
7
8
9
10
11
19
18
17
16
15
14
13

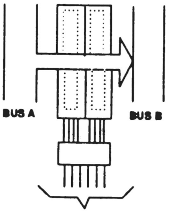
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'ALS646/'ALS646-1 and 'ALS648/'ALS648-1. The select pins determine whether data is stored or transferred through the device in real time. The DIR determines which bus will receive data when the $\overline{OE}$ pin is Low.

REAL TIME BUS TRANSFER
BUS B TO BUS A



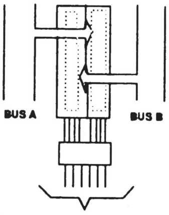
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER
BUS A TO BUS B



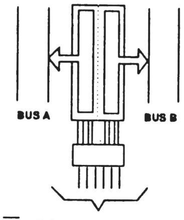
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	H	X	X	L	X

STORAGE FROM
A, B, OR A AND B



$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

TRANSFER STORED DATA
TO A OR B



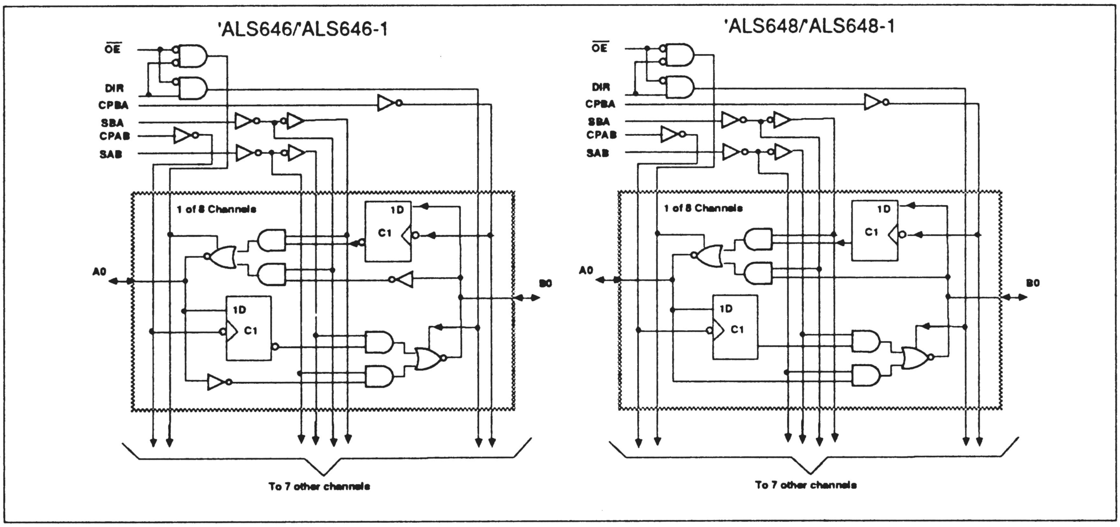
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	'ALS646/'ALS646-1	'ALS648/'ALS648-1
X	X	↑	X	X	X	Input	Unspec*	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Unspec*	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			Stored B data to A bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			Store A data to B bus	Stored $\overline{A}$ data to B bus

H= High voltage level
L= Low voltage level
*= The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
↑ =Low-to-High clock transition
X=Don't care

LOGIC DIAGRAM


'ALS646/'ALS646-1
$\overline{OE}$
DIR
CPBA
SBA
CPAB
SAB
1 of 8 Channels
1D
C1
1D
C1
A0
B0
To 7 other channels
'ALS648/'ALS648-1
$\overline{OE}$
DIR
CPBA
SBA
CPAB
SAB
1 of 8 Channels
1D
C1
1D
C1
A0
B0
To 7 other channels

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state (All versions)	48	mA
I_{OUT}	Current applied to output in Low output state (-1 version)	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version			48[1]	mA
T_A	Operating free-air temperature range		0		70	°C

1. The 48 mA limit applies only under the condition of V_{CC}=5.0V±5%.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} ± 10%	V_{IL} = MAX V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} -2			V
				V_{CC} = MIN		I_{OH} = -3mA	2.4	3.2		V
						I_{OH} = -15mA	2.0			V
V_{OL}	Low-level output voltage	All versions		V_{CC} = MIN	V_{IL} = MAX V_{IH} = MIN	I_{OL} = 12mA		0.25	0.4	V
						I_{OL} = 24mA		0.35	0.5	V
		-1 version		V_{CC} = 4.75V		I_{OL} = 48mA		0.35	0.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	Control inputs		V_{CC} = MAX, V_I = 7.0V					0.1	mA
		A or B ports		V_{CC} = MAX, V_I = 5.5V					0.1	mA
I_{IH}	High-level input current[3]			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current[3]			V_{CC} = MAX, V_I = 0.4V					-0.2	mA
I_O	Short-circuit output current[4]			V_{CC} = MAX,V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	'ALS646 'ALS646-1	I_{CCH}	V_{CC} = MAX				47	76	mA
			I_{CCL}					55	88	mA
			I_{CCZ}					55	88	mA
		'ALS648 'ALS648-1	I_{CCH}					47	76	mA
			I_{CCL}					57	88	mA
			I_{CCZ}					57	88	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS for 'ALS646/'ALS646-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	40		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to B_n or A_n	Waveform 1	10 5	30 17	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2, 3	5 3	20 12	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n or SAB to B_n (A or B Low)	Waveform 2, 3	15 5	35 20	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n or SAB to B_n (A or B High)	Waveform 2, 3	8 5	25 20	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	3 5	17 20	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	1 2	10 16	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	10 5	30 25	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	1 2	10 16	ns

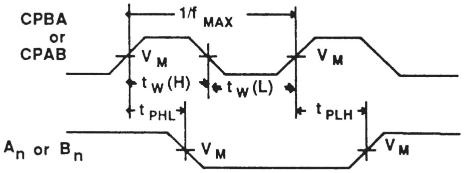
AC ELECTRICAL CHARACTERISTICS for 'ALS648/'ALS648-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	40		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to B_n or A_n	Waveform 1	8 5	30 20	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2, 3	3 2	17 10	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n or SAB to B_n (A or B Low)	Waveform 2, 3	5 4	39 22	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n or SAB to B_n (A or B High)	Waveform 2, 3	6 6	25 21	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	4 4	22 22	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	1 2	10 15	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	4 3	27 19	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	1 2	14 15	ns

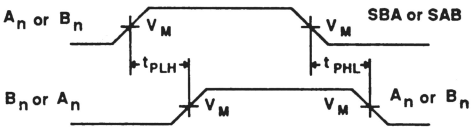
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	10 10		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	12.5 12.5		ns

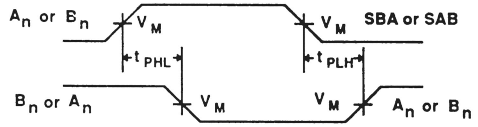
AC WAVEFORMS


CPBA
or
CPAB
1/f MAX
V M
V M
t W(H)
t W(L)
t PHL
t PLH
A n or B n
V M
V M

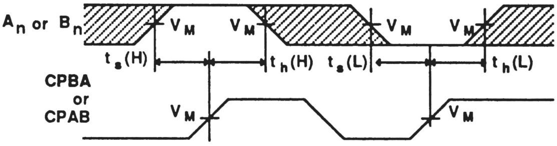
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


A n or B n
V M
V M
SBA or SAB
t PLH
t PHL
B n or A n
V M
V M
A n or B n

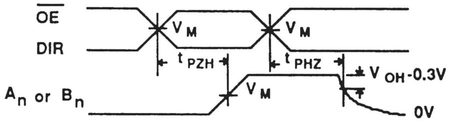
Waveform 2. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn


A n or B n
V M
V M
SBA or SAB
t PHL
t PLH
B n or A n
V M
V M
A n or B n

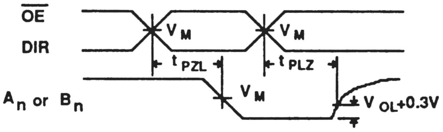
Waveform 3. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn


A n or B n
V M
V M
V M
V M
t s(H)
t h(H)
t s(L)
t h(L)
CPBA
or
CPAB
V M
V M

Waveform 4. Data Setup And Hold Times


OE
DIR
V M
V M
t PZH
t PHZ
V OH-0.3V
A n or B n
V M
0V

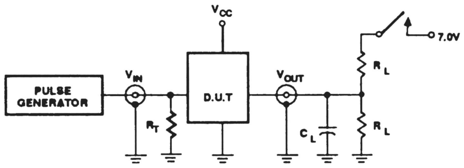
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level


OE
DIR
V M
V M
t PZL
t PLZ
A n or B n
V M
V OL+0.3V

Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_{CC}
7.0V
PULSE GENERATOR
V_{IN}
R_T
D.U.T
V_{OUT}
C_L
R_L
R_L

Test Circuit For 3-State and Open Collector Outputs

SWITCH POSITION

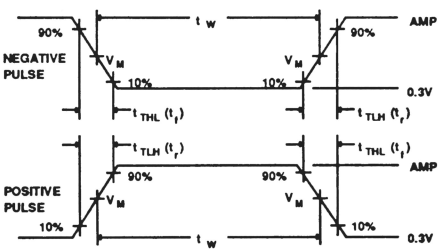
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
V_M
10%
t_W
AMP
0.3V
t_{THL} (t_f)
t_{TLH} (t_r)
POSITIVE PULSE
90%
V_M
10%
t_{TLH} (t_r)
t_{THL} (t_f)
t_W
AMP
0.3V

V_M = 1.3V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

74ALS651, 74ALS651-1
74ALS652, 74ALS652-1
Transceivers/Registers

74ALS651/651-1 Octal Transceiver/Register, Inverting (3-state)
74ALS652/652-1 Octal Transceiver/Register, Non-Inverting (3-state)
Preliminary Specification

FEATURES

- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-state outputs**
- **The -1 version sinks 48mA I_{OL} within the ±5% V_{CC} range**

DESCRIPTION

The 74ALS651 and 74ALS652 Transceivers/ Registers consist of bus transceiver circuits with 3-state outputs , D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{\text{OEBA}}$) and Select (SAB, SBA) pins are provided for bus management. The 74ALS651-1 and 74ALS652-1 will sink 48mA if the V_{CC} is limited to 5.0V±0.25V.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS651/651-1	50MHz	48mA
74ALS652/652-1	50MHz	50mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Dip	74ALS651N,74ALS651-1N,74ALS652N,74ALS652-1N
24-Pin Plastic SOL	74ALS651D,74ALS651-1D,74ALS652D,74ALS652-1D

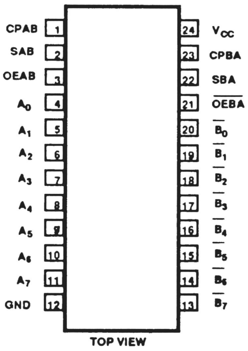
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	1.0/2.0	20µA/0.2mA
B_0 - B_7	B inputs	1.0/2.0	20µA/0.2mA
CPAB	A-to-B clock input	1.0/2.0	20µA/0.2mA
CPBA	B-to-A clock input	1.0/2.0	20µA/0.2mA
SAB	A-to-B select input	1.0/2.0	20µA/0.2mA
SBA	B-to-A select input	1.0/2.0	20µA/0.2mA
OEAB	A-to-B output enable input	1.0/2.0	20µA/0.2mA
$\overline{\text{OEBA}}$	B-to-A output enable input	1.0/2.0	20µA/0.2mA
A_n, B_n	Outputs	750/240	15mA/24mA
A_n, B_n	Outputs (-1 version)	750/480	15mA/48mA

NOTE:
One (1.0) ALS Unit Load is defined as: 20µA in the High state and 0.1mA in the Low state.

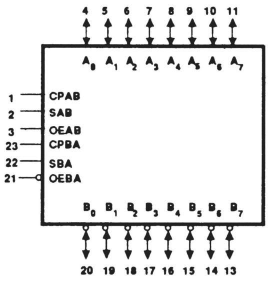
PIN CONFIGURATION

'ALS651/'ALS651-1


CPAB 1
SAB 2
OEAB 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
GND 12
24 VCC
23 CPBA
22 SBA
21 OEBA
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
TOP VIEW

LOGIC SYMBOL

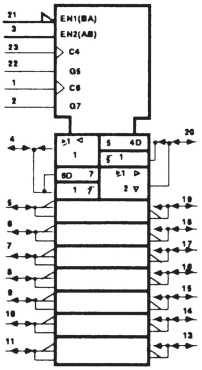
'ALS651/'ALS651-1


4 5 6 7 8 9 10 11
A0 A1 A2 A3 A4 A5 A6 A7
1 CPAB
2 SAB
3 OEAB
23 CPBA
22 SBA
21 OEBA
B0 B1 B2 B3 B4 B5 B6 B7
20 19 18 17 16 15 14 13

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

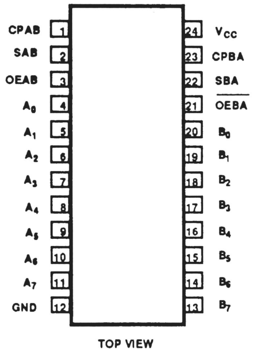
'ALS651/'ALS651-1


21
3
23
22
1
2
EN1(BA)
EN2(AB)
C4
G5
C6
G7
4
20
≥1
1
5
4D
6D
7
≥1
2
5
6
7
8
9
10
11
19
18
17
16
15
14
13

October 12, 1988

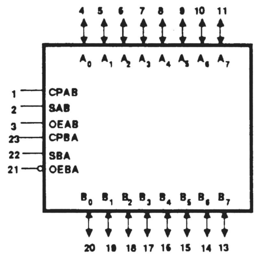
PIN CONFIGURATION

'ALS652/'ALS652-1


CPAB 1
SAB 2
OEAB 3
A0 4
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
GND 12
24 VCC
23 CPBA
22 SBA
21 OEBA
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
TOP VIEW

LOGIC SYMBOL

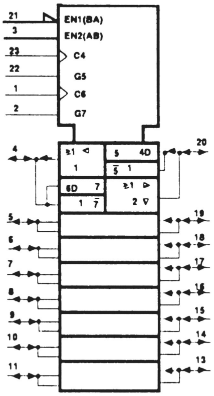
'ALS652/'ALS652-1


4 5 6 7 8 9 10 11
A0 A1 A2 A3 A4 A5 A6 A7
1 CPAB
2 SAB
3 OEAB
23 CPBA
22 SBA
21 OEBA
B0 B1 B2 B3 B4 B5 B6 B7
20 19 18 17 16 15 14 13

V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'ALS652/'ALS652-1

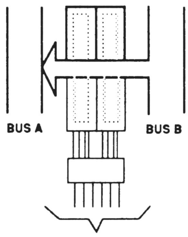

21
3
23
22
1
2
EN1(BA)
EN2(AB)
C4
G5
C6
G7
≥1
1
5 4D
5 1
6D 7
1 7
≥1
2
4
5
6
7
8
9
10
11
20
19
18
17
16
15
14
13

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'ALS651/'ALS651-1 and 'ALS652/'ALS652-1.

The select pins determine whether data is stored or transferred through the device in real time.

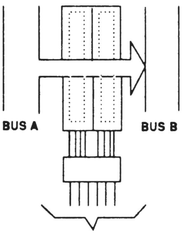
The output enable pins determine the direction of the data flow.

REAL TIME BUS TRANSFER BUS B TO BUS A



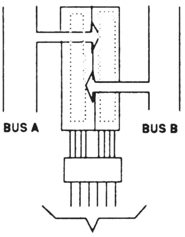
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



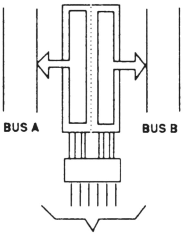
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA	An	Bn	'ALS651/'ALS651-1	'ALS652/'ALS652-1
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified output *	Store A, Hold B	Store A, Hold B
H	H	↑	↑	**	X			Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified output *	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	**			Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{\text{B}}$ data to A bus	Real time B data to A bus
L	L	X	H or L	X	H			Stored $\overline{\text{B}}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{\text{A}}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X			Stored $\overline{\text{A}}$ data to B bus	Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{\text{A}}$ data to B bus Stored $\overline{\text{B}}$ data to A bus	Stored A data to B bus Stored B data to A bus

H= High voltage level

L= Low voltage level

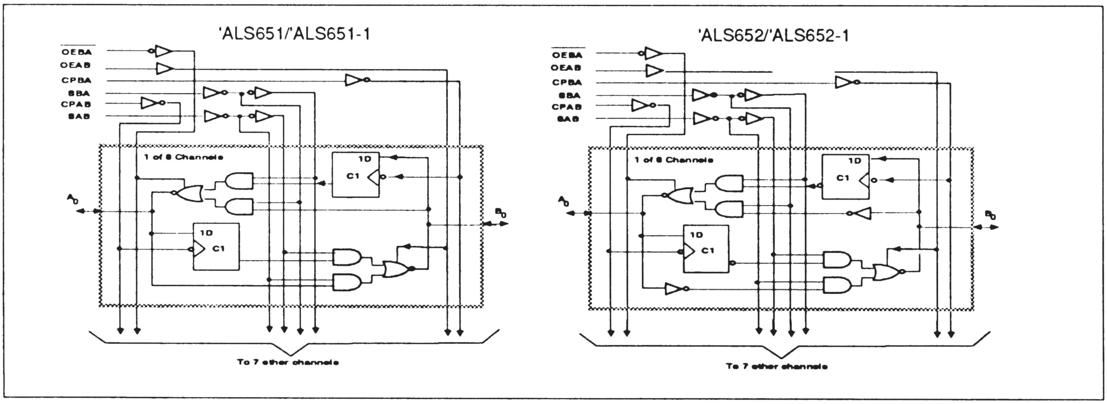
*= The data output function may be enabled or disabled by various signals at the $\overline{\text{OEBA}}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

↑ =Low-to-High clock transition

X=Don't care

** If Select control = L, then clocks can occur simultaneously. If Select control = H, the clocks must be staggered in order to load both registers.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state (All versions)	48	mA
I_{OUT}	Current applied to output in Low output state (-1 version)	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version			48[1]	mA
T_A	Operating free-air temperature range		0		70	°C

1. The 48 mA limit applies only under the condition of V_{CC}=5.0V±5%.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} ± 10%	V_{IL} = MAX V_{IH} = MIN	I_{OH} = -0.4mA	V_{CC} -2			V
				V_{CC} = MIN		I_{OH} = -3mA	2.4	3.2		V
						I_{OH} = -15mA	2.0			V
V_{OL}	Low-level output voltage	All versions		V_{CC} = MIN	V_{IL} = MAX V_{IH} = MIN	I_{OL} = 12mA		0.25	0.4	V
						I_{OL} = 24mA		0.35	0.5	V
		-1 version		V_{CC} = 4.75V		I_{OL} = 48mA		0.35	0.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	Control inputs		V_{CC} = MAX, V_I = 7.0V					0.1	mA
		A or B ports		V_{CC} = MAX, V_I = 5.5V					0.1	mA
I_{IH}	High-level input current[3]			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current[3]			V_{CC} = MAX, V_I = 0.4V					-0.2	mA
I_O	Short-circuit output current[4]			V_{CC} = MAX, V_O = 2.25V			-30		-112	mA
I_{CC}	Supply current (total)	'ALS651 'ALS651-1	I_{CCH}	V_{CC} = MAX				42	68	mA
			I_{CCL}					52	82	mA
			I_{CCZ}					52	82	mA
		'ALS652 'ALS652-1	I_{CCH}					47	76	mA
			I_{CCL}					55	88	mA
			I_{CCZ}					55	88	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS for 'ALS651/'ALS651-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	40		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to B_n or A_n	Waveform 1	10 5	32 17	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 3, 4	4 2	18 10	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n or SAB to B_n (A or B Low)	Waveform 3, 4	13 7	38 21	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n or SAB to B_n (A or B High)	Waveform 3, 4	8 7	25 21	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to A_n	Waveform 8 Waveform 9	5 5	20 18	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to A_n	Waveform 8 Waveform 9	2 3	9 12	ns
t_{PZH} t_{PZL}	Output Enable time OEAB to B_n	Waveform 8 Waveform 9	7 7	22 21	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB to B_n	Waveform 8 Waveform 9	2 2	12 14	ns

AC ELECTRICAL CHARACTERISTICS for 'ALS652/'ALS652-1

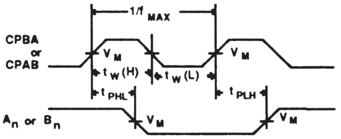
SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	40		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to B_n or A_n	Waveform 1	10 5	30 17	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 3, 4	5 3	18 12	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n or SAB to B_n (A or B Low)	Waveform 3, 4	15 6	35 20	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n or SAB to B_n (A or B High)	Waveform 3, 4	8 5	25 20	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to A_n	Waveform 8 Waveform 9	3 5	17 18	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to A_n	Waveform 8 Waveform 9	1 2	10 16	ns
t_{PZH} t_{PZL}	Output Enable time OEAB to B_n	Waveform 8 Waveform 9	8 6	22 18	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB to B_n	Waveform 8 Waveform 9	1 2	10 16	ns

AC SETUP REQUIREMENTS

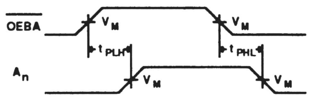
SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		UNIT
			Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 5	10 10		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 5	0 0		ns
t_s(H) t_s(L)	Setup time, High or Low ^{1} $\overline{\text{OEBA}}$ to OEAB or OEAB to $\overline{\text{OEBA}}$	Waveform 6, 7	10 10		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{\text{OEBA}}$ to OEAB or OEAB to $\overline{\text{OEBA}}$	Waveform 6, 7	0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	12.5 12.5		ns

Note : 1. Setup time is to protect against current surge caused by enabling 16 outputs (24mA per output) simultaneously.

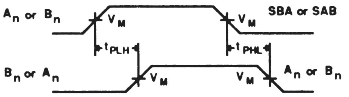
AC WAVEFORMS


1/f MAX
CPBA or CPAB
V_M
t_W(H)
t_W(L)
t_{PHL}
t_{PLH}
A_n or B_n

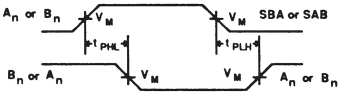
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency


$\overline{\text{OEBA}}$
V_M
t_{PLH}
t_{PHL}
A_n

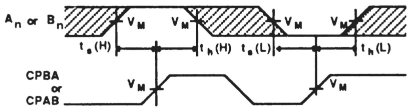
Waveform 2. Enable and disable times for open collector outputs


A_n or B_n
SBA or SAB
V_M
t_{PLH}
t_{PHL}
B_n or A_n
A_n or B_n

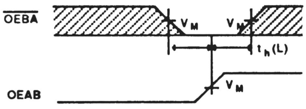
Waveform 3. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn


A_n or B_n
SBA or SAB
V_M
t_{PHL}
t_{PLH}
B_n or A_n
A_n or B_n

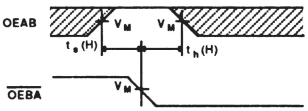
Waveform 4. Propagation Delay, An or Bn to Bn or An and SBA or SAB to An or Bn


A_n or B_n
V_M
t_s(H)
t_h(H)
t_s(L)
t_h(L)
CPBA or CPAB

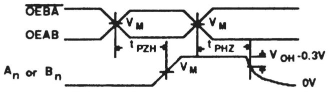
Waveform 5. Data Setup And Hold Times


$\overline{\text{OEBA}}$
V_M
t_h(L)
OEAB

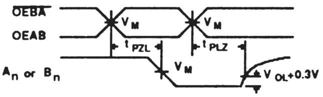
Waveform 6. $\overline{\text{OEBA}}$ to OEAB Setup And Hold Times


OEAB
V_M
t_s(H)
t_h(H)
$\overline{\text{OEBA}}$

Waveform 7. OEAB to $\overline{\text{OEBA}}$ Setup And Hold Times


$\overline{\text{OEBA}}$
OEAB
V_M
t_{PZH}
t_{PHZ}
V_{OH}-0.3V
0V
A_n or B_n

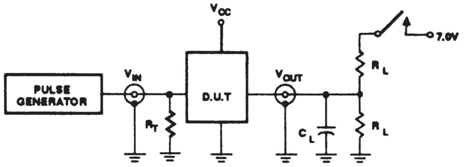
Waveform 8. 3-State Output Enable Time To High Level And Output Disable Time From High Level


$\overline{\text{OEBA}}$
OEAB
V_M
t_{PZL}
t_{PLZ}
V_{OL}+0.3V
A_n or B_n

Waveform 9. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS


V_CC
7.0V
PULSE GENERATOR
V_IN
R_T
D.U.T
V_OUT
C_L
R_L
R_L

Test Circuit For 3-State and Open Collector Outputs

SWITCH POSITION

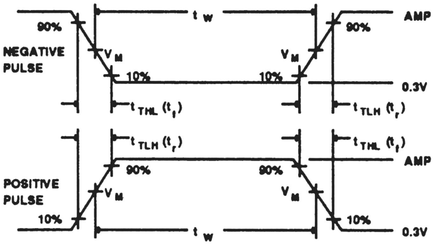
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


NEGATIVE PULSE
90%
V_M
10%
t_W
t_THL (t_f)
t_TLH (t_r)
AMP
0.3V
POSITIVE PULSE
90%
V_M
10%
t_TLH (t_r)
t_THL (t_f)
AMP
0.3V

$V_M = 1.3V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	**Rep. Rate**	t_W	t_{TLH}	t_{THL}
74ALS	3.5V	1MHz	500ns	2.0ns	2.0ns

Section 6
ALS Application Note

INDEX

AN203 Test Fixtures for High–Speed Logic 6–3

AN203

Test Fixtures for High-Speed Logic

Application Note

INTRODUCTION

The Signetics Standard Products Division (SPD) operates a Characterization Laboratory in Orem, Utah. This Lab maintains the capability of testing the 11 logic product families the Division supports. These include: AuTTL-74XXX, Schottky-74SXXX, Low-Power Schottky-74LSXXX, FAST-74FXXX, ALS-74ALSXXX, High-Speed CMOS-74HCXXX, High-Speed CMOS/TTL-74HCTXXX, Advanced CMOS/TTL (ACL)-74ACT11XXX, Advanced CMOS (ACL)-74AC11XXX, and both 10K and 100K ECL.

Due to the great diversity of product families and the different testing requirements and complexity of the product types of each family, Signetics SPD Characterization has designed and built a bench test AC fixture that is specifically designed to address to only the High-speed logic families. It has the advantages of being very versatile, has high bandwidth capability ($\geqslant$750MHz), is 50Ω system compatible, and is manually programmable for the input static voltages. This provides the ability to have one fixture that addresses many product types across families. The extent of this versatility is explained in the following Application Note. The families that this fixture is intended to support are: FAST, ALS, ACL, 10K ECL, and 100K ECL (Note: This fixture is compatible with any 500Ω pulldown load.)

THEORY OF OPERATION

There are several key points in testing the faster edge-rate logic families. They are:

- Very good bypassing and decoupling (they are different).
- Large ground and V_{CC} planes
- Low-impedance signal lines (i.e., 50Ω)
- Signal lines that are uniform in impedance over frequency
- Signal lines must have high bandwidth ($>$ 500MHz)
- Low-inductance paths for the DUT leads, including V_{CC} and GND
- Output AC load close to the DUT
- Measurement point close to the DUT
- Avoidance of ground loops (especially on inputs at DC levels)

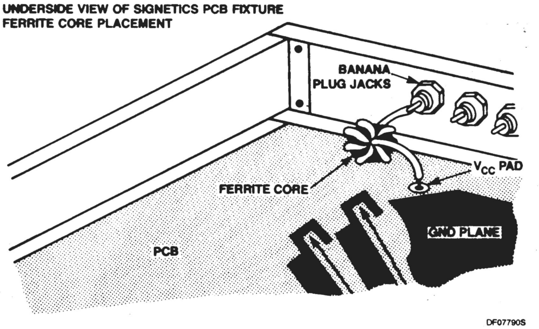


Figure 1. Ferrite Core Placement

Additional items of concern to the test engineer and the manager are:

- Versatility and/or ease of use (there are trade-offs)
- Cost
- The number of fixtures needed to support products

Each of these concerns have merit and must be understood by the user of these logic families if valid and correlatable results are to be found.

V_{CC} and GND

The secret in V_{CC} and GND use in fixturing is to do the things that reduce the noise that can: 1) get to your part, and 2) come from your part. This is done by reducing the noise of the V_{CC} as it arrives to the fixture, by judicious application of frequency dependant bypassing at the DUT V_{CC} pin to GND and reducing inductance from the V_{CC} and GND pins of the DUT to the point where good contact of the bypassing and V_{CC} and GND planes occur. All of these are techniques used in good RF and microwave board design. By reducing parasitic inductances and cleaning up any sources of noise, good signal integrity is better maintained.

These points are evident in the fixture Signetics has designed. Part of the noise reduction of the power supply as it arrives is done by bypassing the power supply at its terminals. The power is then brought to the fixture via banana cables, (as short as possible), to jacks on the chassis of the fixture. An 18 gauge wire, attached to the jack, is wrapped through a ¾ inch ferrite core 8 to 12 times for decoupling of any spikes. (Details of the cores used are included in the parts list.) This acts as a Low-pass filter. The wire is then soldered to the bottom of the PC board onto the large V_{CC} plane that narrows to the V_{CC} bus running between the pins of the DUT. See Figures 1 and 2 for detail.

Triangle-shaped, the V_{CC} plane provides a Low inductive path for the V_{CC} to the DUT pin. See Figure 2 for the board layouts. The V_{CC} bus from this plane travels down between the DUT pins to that connection. This is so connection to the V_{CC} bus is easy and very short. The DUT may have V_{CC} located on any pin with this configuration. The pin is connected to the V_{CC} bus by soldering small copper braid or similar Low-inductance wire capable of carrying the current for the device, see Figure 3.

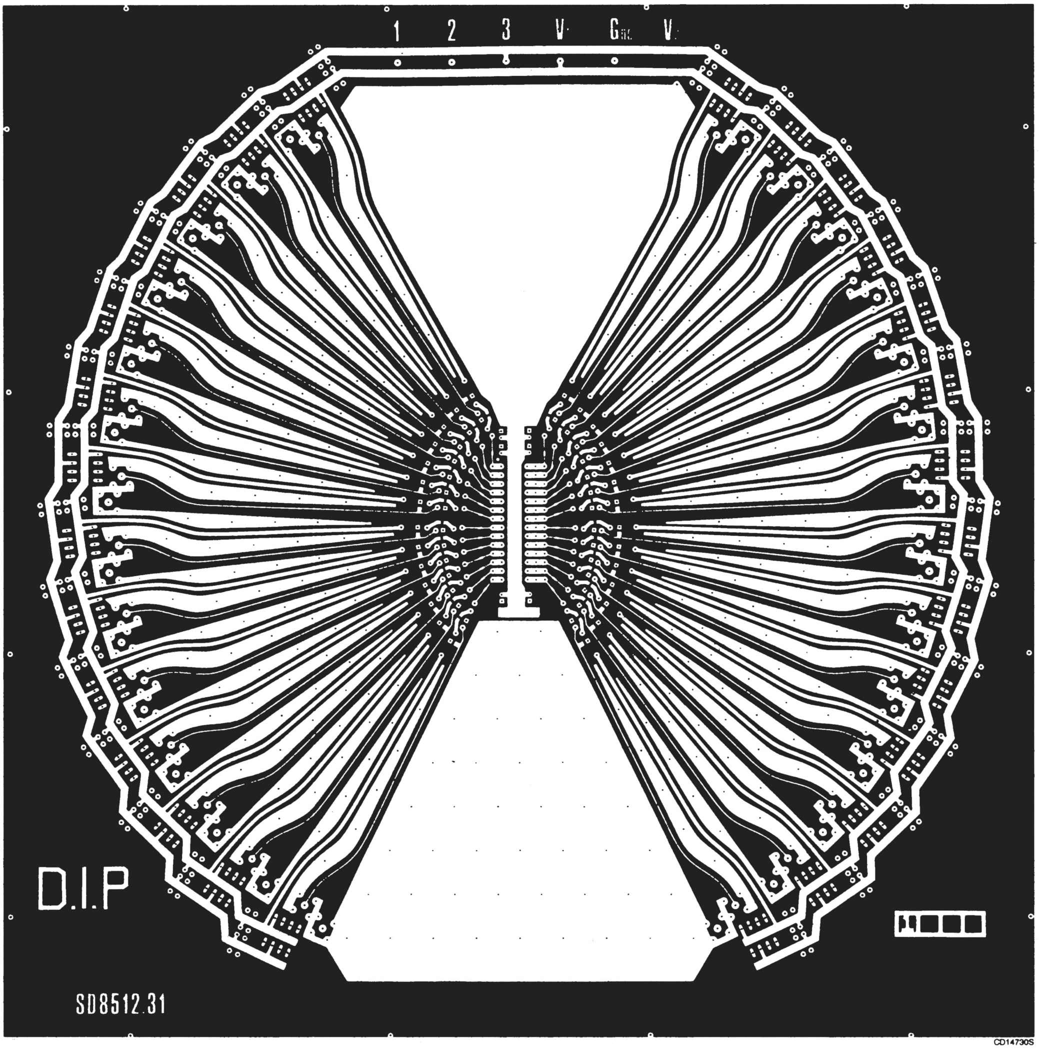

1
2
3
V-
Gnd
V+
D.I.P
SD8512.31
CD14730S

Figure 2a. Board Layout - Top Side

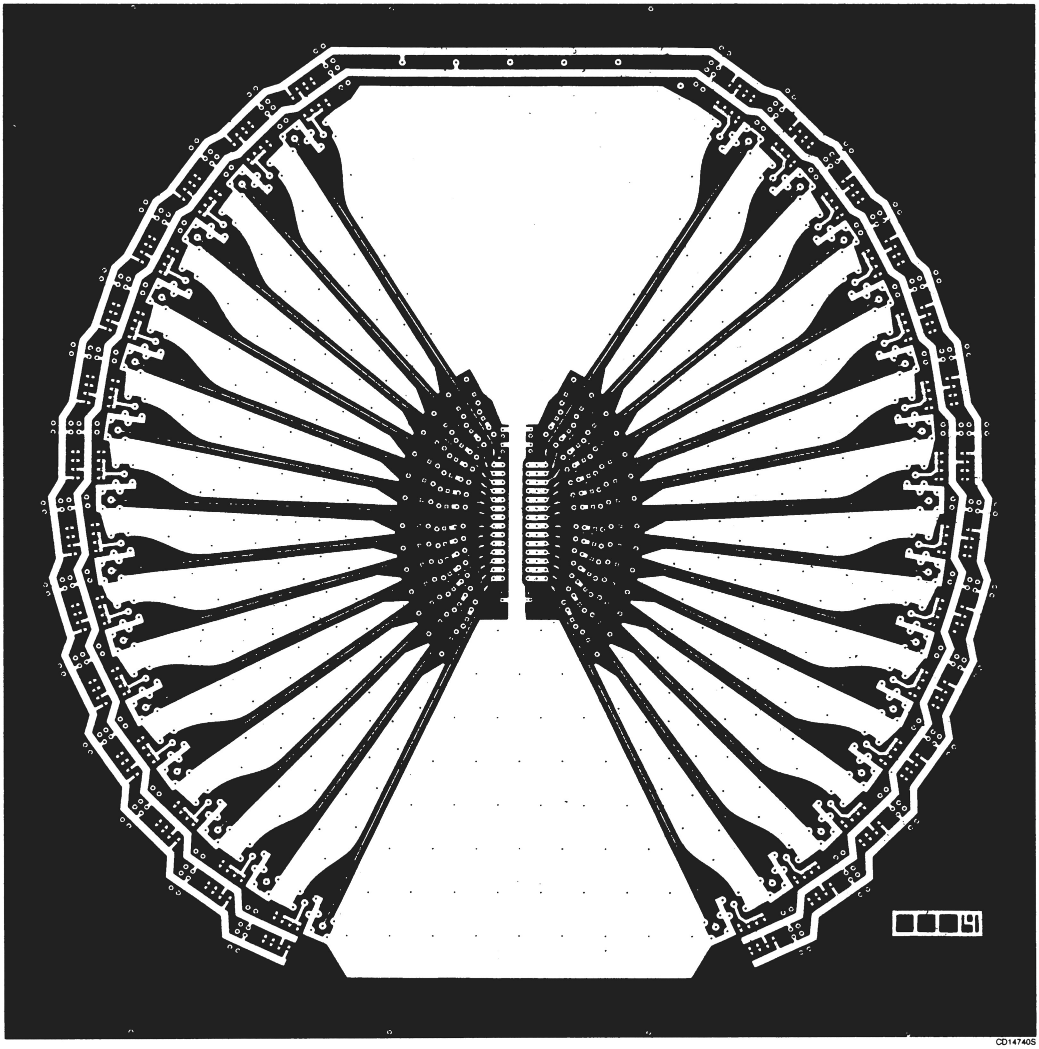


Figure 2b. Board Layout - Bottom Side

On the opposite side of the top layer of the board is a triangle-shaped ground plane. Ground planes are also located on the bottom layer of the board in the same places as the V_{CC} and ground planes of the top layer. Since this fixture is laid out for 50Ω stripline, layers 2 and 3 are almost total ground plane, with holes in them for feed-throughs and components. Also found between the signal lines, on the top and bottom layers, are ground plane "fingers" that are connected to all 4 layers by plated-through holes. This provides good separation of the signal lines resulting in lower crosstalk.

The bottom layer ground plane consists of two triangle-shaped planes connected by a bus strip that runs between the DUT pins. This was done for 3 reasons: First, this allows connection of any ground pin of the DUT to the ground, regardless of location; like the V_{CC} connection on the top layer. Second, it allows the connection of the bypass capacitors from the V_{CC} pin to the ground with the shortest possible lead length. Characterization uses typically 2 or 3 ceramic chip capacitors and 1 or 2 dipped tantalum capacitors (35V) to bypass the V_{CC} pin. It is important to keep the dipped tantalum capacitor's leads as short as possible to reduce series inductance. The recommended values of capacitors are: 100pf, .01μf, .1μf. and 10μf. We have found at times, the need to adjust these values depending upon the product type and its performance. Some noise sensitive circuits need more bypassing in the lower and extreme higher values of capacitance. And third, the connection of the two planes eliminates possible ground loops and the feed-throughs create a ground mesh and give an excellent ground plane for the circuit. Figure 3 illustrates the bypass connections.

BYPASS AND DECOUPLING

It is important to understand the difference between decoupling, as with the ferrite core, and bypassing, as with capacitors. Decoupling occurs as or high-frequency signals are removed by saturation of the ferrite core. This prevents "noise" that may be on the V_{CC} power supply from getting on the V_{CC} plane. The action of the bypassing capacitors is to: 1) "pass" any non-DC signals that occur on the V_{CC} (due to the part's operation) to ground, and 2) be able to provide the "instantaneous" current demands of the part as it switches.

The various values of capacitors are intended to provide a Low-impedance path at all operating frequencies. Since real-world capacitors have resonance points at a given frequency, depending upon their value and type of capacitor (and actually turn inductive above the resonance point), using different values that have different resonance points allows an across-frequency Low-impedance path for V_{CC} noise.

An important point in the use of bypass capacitors is the minimization of lead length. Lead length represents inductance; inductance in series with the capacitance. If it is too much, it can cause resonance and oscillation problems with the part and/or power supplies and nullify the benefit of the capacitors. It also plays a major part in inhibiting the effect of the "instantaneous" current response needed by the part from the bypass capacitors. It actually can cause the ground of the device to track the change in current to the degree of the lead inductance. The lower the inductance, the lower the "ground bounce" effect. Hence, short or no lead lengths on capacitors are needed to help prevent the effects of ground bounce.

SIGNAL LINES

A signal line is defined as a line that carries the input stimulus, either DC or AC, or output response, to or from the device. Since these signals are measured and determine the data which characterizes the part, it is critical that they are of the highest integrity and represent, as far as physically possible, the action of the part; not the nuances of the fixture. To achieve this, the line must not be able to change the signal over the measureable frequencies of the device, nor affect the delay of the part.

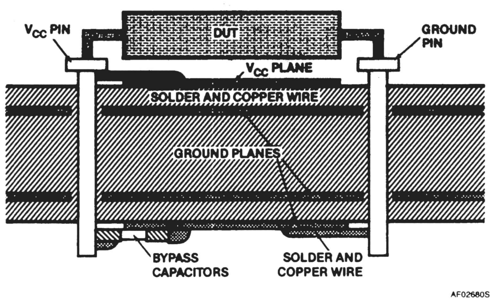


Figure 3. Decoupling Connections

The fixture as designed, has 50Ω signal lines determined by a stripline layout method. The 50Ω value was selected for several reasons: 1) the 50Ω value matches impedance with the pulse generators that are used as input stimulus. 2) The output loads specified for this fixture are either a 500Ω pulldown or a 50Ω pulldown (ECL), in parallel with a capacitive load. This allows the 50Ω signal line to be terminated into this load for either a 10:1 or a 1:1 match. 3) A Low-impedance line will have better characteristics with regards to crosstalk and resisting external noise.

There are two types of signal lines on this fixture: input and output; both of which are 50Ω transmission lines. The input line is on the top side of the board and is always terminated in 50Ω. It is connected to the DUT via a .3″ jumper, Jumper #1 for input. When this jumper is installed, the DUT pin is available only as an input. To allow this line to be used as an output, a .1″ jumper, Jumper #1 for output, is used instead of the .3″ jumper. This connects the DUT pin to the AC load when the DUP pin is an output. See Figure 5.

The output signal line can be dedicated two different ways. The first method, used for ECL, is to leave shorted the 50Ω trace and have it run directly into the SMB connector into the 50Ω sampling system. The second method is to cut the trace at the DUT pin and solder the 450Ω chip resistor, R1, across the cut. This, combined with the 50Ω scope, then appears to the part as either a 500Ω probe for the input signal or the 500Ω output AC load for the output signal.

The signal lines are equal length and therefore do not introduce any extraneous delay from pin to pin. We also characterized the impedance of the lines over frequency to ensure minimal distortion over the frequency range and any effective change in propagation delay caused by the relationship of inductance and group delay. Figure 4 illustrates the frequency response of the signal lines in impedance.

This is considered to be high bandwith and encompasses the frequency range exhibited by ALS, ACL, ELC, and FAST logic families.

Test Fixtures for High-Speed Logic

AN203

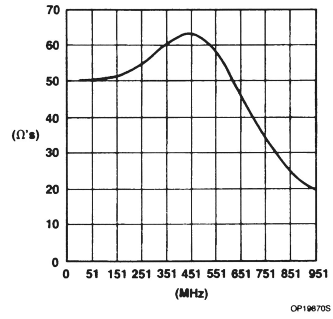


Figure 4. Signal Line Frequency Response

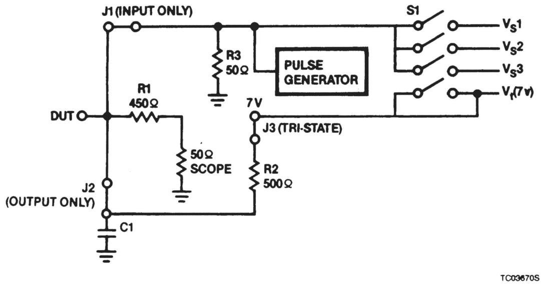


Figure 5. Signetics PCB Fixture Schemetic

LOADING

The explanation of the two types of AC loads that may be used will be covered in two parts. First the ALS, ACL, and FAST implementation will be discussed, then the ECL implementation.

ALS. ACL, and FAST Implementation

The FAST, ALS, and ACL product families AC load is specified as a 50pF capacitor and a 500Ω resistor in parallel. This load has the advantage of being adaptable to both a High-impedance (A.T.E.) or a Low-impedance (bench) measurement environment. The Signetics fixture uses a Low-impedance environment primarily for two reasons. The first reason is that experience of the last 5 years has told us that High-impedance probes represent a reliability concern and can introduce hard to detect errors into the waveform. The second reason being that most suppliers of these technologies provide data based upon the Low-impedance approach and most large users of these products do so as well. This also allows the fixture to be used for ECL testing since that product uses a totally 50Ω environment. Figure 5 illustrates how this test fixture implements the 50pF/500Ω load schematically.

The fixture was laid out to present the load as close as possible to the device, and yet allow for flexibility in deciding if a certain pin is an output or an input. This distance is critical due to its inductive effect upon ground bounce phenomena. *It is acknowledged here that a fixture dedicated to a single device type without jumpers, and therefore placing the load virtually on the pin of the device, would show the ground bounce phenomena for simultaneous switching to be less than that of this fixture. However, this fixture can be so dedicated by not using the pads as provided, but rather by using the ground bus, like the bypass capacitors used. The flexibility of this fixture substantially reduces the cost of fixturing for these families. Studies on simultaneous switching with this fixture have shown dramatically favorable results to previous fixtures. Those studies continue. For work other than that of simultaneous switching, there will be no appreciable difference with a dedicated fixture.*

As illustrated in Figure 5, the load is shared with the 50Ω input of the measurement system; a 50Ω sampling oscilloscope. The 450Ω resistor: R1, is soldered to the socket pin of the device and is in series with the 50Ω input of the scope. Figure 6 illustrates this on the board layout of one input/output pin. This allows virtually a probe tip on the device pin. The load capacitor: C1, is a 33pF ceramic chip capacitor. This is added to the measured value of 17pF of board capacitance, achieving the 50pF value specified for the load. The distance from the pin to the capacitor is .5 inches and is adequate for the testing of these product families.

For testing 3-State parameters, the 500Ω resistor: R2, is connected to it's pullup supply. V_t via a .3" jumper: Jumper #2. The V_t supply is bussed to each pin and may or may not be connected with that jumper. See Figures 5 and 6.

ECL Implementation

When testing ECL product, the 450Ω resistor: R1, is not used, Rather, this point is left shorted together in the construction process. Also for ECL, the load chip capacitor: C1, the tri-state pull-up resistor: R2, the 50Ω terminator: R3, and the "output only" jumper: Jumper #1, are not used. The input signal travels down the input path, is jumpered using the "input only" (Jumper #1), goes to the device, travels out the output path (left shorted, no R1), and proceeds to the scope. When the signal is an output, the "input only" jumper: Jumper #1, is removed and a 50Ω terminator is connected to the SMB connector as the load or the 50Ω input of the scope. See Figure 7.

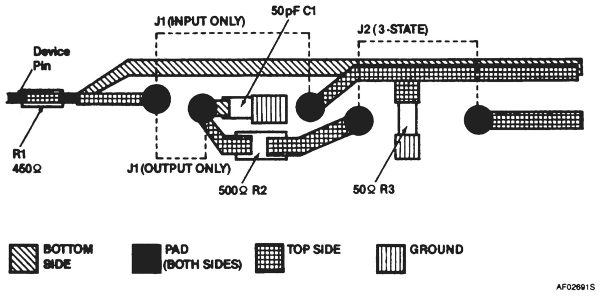

50pF C1
J1 (INPUT ONLY)
J2 (3-STATE)
Device Pin
R1
450Ω
J1 (OUTPUT ONLY)
500Ω R2
50Ω R3
BOTTOM SIDE
PAD (BOTH SIDES)
TOP SIDE
GROUND
AF02691S

Figure 6. Signetics Fixture - Board

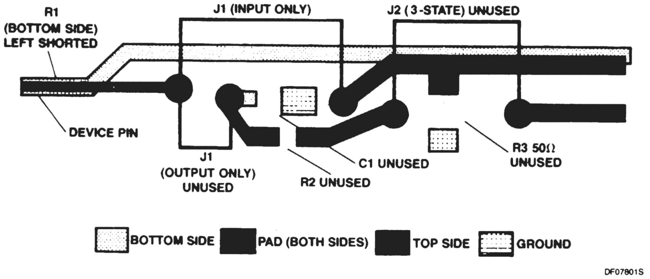

R1
(BOTTOM SIDE)
LEFT SHORTED
J1 (INPUT ONLY)
J2 (3-STATE) UNUSED
DEVICE PIN
J1
(OUTPUT ONLY)
UNUSED
C1 UNUSED
R2 UNUSED
R3 50Ω
UNUSED
BOTTOM SIDE
PAD (BOTH SIDES)
TOP SIDE
GROUND
DF07801S

Figure 7. ECL Configuration

INPUT STIMULUS AND MEASUREMENT

When the input is not used for a signal input, the line may be switched to one of three voltage sources: V_s 1 through V_s 3, by the use of a DIP switch on each pin. It may also be left open and then the 50Ω pulldown resistor: R1, pulls the line to ground and can be used as a hard low level. See Figure 5. These voltage levels are brought in from external supplies through banana connectors like V_{CC}. This scheme eliminates excessive cabling to each input to provide the static input levels and thereby reduces parasitic inductances and cross-talk. Each of the 3 busses and the V_t bus all have places for bypass capacitors in the event of noise on the static levels. Figure 8 illustrates the DIP switch and SMB connectors and how they control the input stimulus and output measurement.

As stated previously, the measurements are made with 50Ω sampling systems. The connections to these systems are made via SMB connectors. This was chosen since it is compatible with SMC; it is push-on, it is small for easy configuration, and it is capable of high bandwidth operation. Figure 8 illustrates where the connections are made, where the pulse generators connect to the input and an SMB connector. Since the 450Ω resistor: R1, is soldered directly to the pin of the device, the actual probe tip is at that point. See Figure 6. This has the advantage of eliminating any distance from the device to the probe tip, thus guaranteeing accurate results.

VERSATILITY AND COST

At some point, there is a choice between the most technically attractive options and the cost of options. This fixture has been primarily designed to optimize the cost effectiveness of test fixturing yet yielding a technically sound tool. To do this, a compromise has been made between the ease of use and the versatility.

In the construction of the fixture, a choice is made as to where the V_{CC} and GND pins are to be located. This then dedicates this particular fixture to part types with this V_{CC} and GND configurations. This is alos done with a dedicated fixture. However, on a dedicated fixture, the pins are individually constructed to be either an input or an output, and in so doing, the fixture is usable for 1-to-4 devices. The Signetics fixture, once dedicated to a particular V_{CC} and GND configuration, is built up to have both input and output components on all signal pins. The selection of which pin is an output or an input is made by inserting the appropriate jumper, See Figures 5 and 6. The same applies in doing tri-state testing. The tradeoff here is that it would probably take less time to setup the dedicated fixture than the Signetics fixture. To help compensate for that tradeoff, we have the three Vs supplies that may be switched into any pin to provide input static levels and eliminate the need to bus input High or Low levels by external cabling. For the user that means the only connections being made to the fixture are:

- the V_{CC} (banana jack)
- the GND (banana jack): this is the common ground of all input supplies.
- the V_S 1, V_S 2, and V_S 3 supplies (banana jack): these may be any voltage and are switchable. Signetics connects programmable supplies to these connectors.
- the V_t supply (banana jack): this is the 3-State pullup voltage and is permanently connected to the bus to each pin. It is selectable by Jumper #2, see Figures 5 and 6. For FAST and ALS products this is 7V. For ACL products this is $V_{CC} \times 2$ and it is not used for ECL applications.
- Input Stimulus (inside SMB connector: this is found on every input/output pin. More than one pin may be used in this manner. **CAUTION:** When using this connector as an input stimulus, make sure V_{S-1}, V_{S-2}, V_{S-3} are disconnected. This will short the power supplies to the generator if they are not disconnected.
- Output Measurement or Scope Connection (outside SMB connector: this is also found on every input/output pin. More than one pin may be used in this manner. Remember, if this pin is not connected to a scope and is an output, a 50Ω resistor must be connected here to ground to complete the 50Ω resistive load. Signetics has constructed 50Ω load by soldering a high-quality (High-frequency) 50Ω resistor inside a female SMB cable connector. See Figure 9.

CAUTION: V_{S-1}, V_{S-2}, and V_{S-3} are all on the same DIP switch. Since they connect to the same bus per pin, **ONLY ONE SUPPLY MAY BE CONNECTED AT ONE TIME**, Otherwise, this will result in a short between power supplies connected.

With these 6 connections, the fixture is capable of testing the product lines as mentioned.

The cost of this fixture ranges from 550 per fixture, dedicated to a 20-pin device in quantities of 1 – 10, to as low as 385 per fixture of the same type in quantities over 100. This is not substantially higher than the cost of a dedicated fixture; which is estimated at 200 – 500. The factor to consider would be the quantity of fixtures for the number of products to be tested. To have a dedicated fixture for every 2 – 3 product types versus a "universal" test fixture for 20 – 30 product types is worth considering from a cost standpoint.

Included in Appendix 1 is the parts list for this fixture and the supplies used by Signetics. This in no way constitutes Signetics endorsements of these suppliers and the customer may select their own supplier if they so desire. This fixture is offerd to the public to duplicate and use within their own environments. Signetics will not provide any materials but will allow the manufacturers of the board and materials to build and/or supply for any requesting party. Pricing and availability are left to the vendors and Signetics has no control over those issues. The intent is to provide something for users of high-speed logic that has been proven and tested in a true high-speed use, and provide a characterization of these products prior to their introduction to the market place.

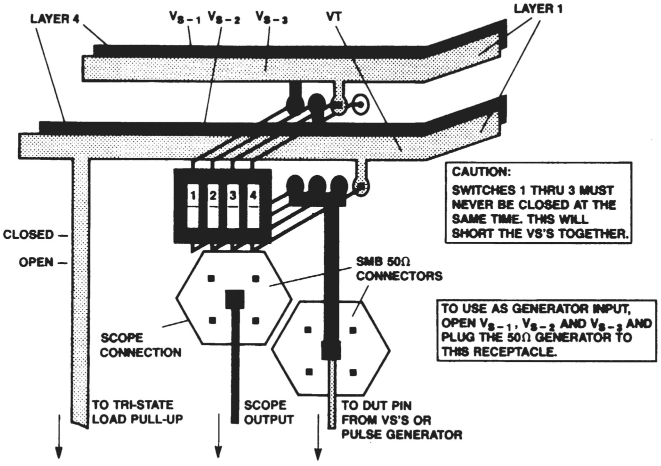

LAYER 4
V_{S-1} V_{S-2} V_{S-3}
VT
LAYER 1
1 2 3 4
CLOSED
OPEN
SMB 50Ω CONNECTORS
SCOPE CONNECTION
TO TRI-STATE LOAD PULL-UP
SCOPE OUTPUT
TO DUT PIN FROM VS'S OR PULSE GENERATOR
CAUTION: SWITCHES 1 THRU 3 MUST NEVER BE CLOSED AT THE SAME TIME. THIS WILL SHORT THE VS'S TOGETHER.
TO USE AS GENERATOR INPUT, OPEN V_{S-1}, V_{S-2} AND V_{S-3} AND PLUG THE 50Ω GENERATOR TO THIS RECEPTACLE.
DF07811S

Figure 8. DIP Switch Connections for V_{S-1}, V_{S-2}, V_{S-3}, and V_T and the SMB Connectors for Input Signals and Output Measurement

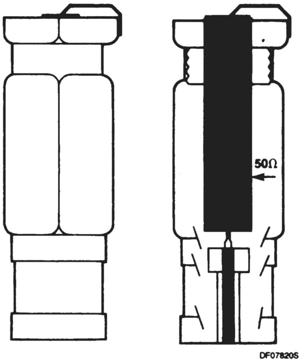

50Ω
DF07820S

Figure 9. 50Ω Load Resistors Using Output Pin SMB Cable Connectors

5. APPENDIX I - Component and Vendor List

The following prices are quoted for a 30 piece build of a 24 pin test fixture and are not binding in any way.

1. Printed circuit mother board.
    - SO and SOL -#SD8512.28
    - DIP -#SD8512.31
    - Requirement: 1 per part configuration

    Supplier: Prototype and Production Circuits
    8040 S. 1444 W.
    West Jordan, UT 84084
    (801) 566-5431

2. SO and SOL sockets.

#_PINS	PART_#
14	001-014
16	001-016
16L	001-116
20	001-120
24	001-124
28	001-128

SOIC through hole socket
Requirement: 1 per board

Supplier: Surface Mount Devices, Inc.
PO Box 16818
Stamford, CT. 06903
(203) 322-8290

3. L$G-1AG14-1 Socket Terminal Pins.
    For DIP boards - number of pins equal to the part pin count times by (7) seven.
    24 × 7 = 160 × .20 =
    For SO and SOL boards - number of pins equal to the part pins count times by (5) five.
    24 × 5 = 120 × .20 =

4. Shorting Blocks (Jumpers).
    .3 inch 8136-475G1 Requirement: 1 per pin
    cost per part × 24 =
    .1 inch 8136-651P2 Requirement: 1 per pin
    cost per part × 24 =

    Supplier: Augat

5. Chip Resistors.
    50Ω 1% CRCW 1210 Requirement: 1 per pin
    cost per part × 24 =
    450Ω 1% CRCW 1206 Requirement: 1 per pin
    cost per part × 24 =
    500Ω 1% CRCW 1206 Requirement: 1 per pin
    cost per part × 24 =

    Supplier: Dale Electronics, Inc.
    2300 Riverside Blvd.
    Norfolk, Nebraska 68701
    (402) 371-0080

6. Chip Capacitors.

Ceramic Part_#	Requirement
33pf 500R15N330JP	1 per bin
cost per part × 24 =	
15pf 500R15N150JP4	1 per board
cost per part × 1 =	
.015μf 500$41W103KP4	1 per board
cost per part × 1 =	
.1μf 500$41W104KP4	1 per board
cost per part × 1 =	

Supplier: Johanson Dielectrics

7. Dipped Tantalum.

Ceramic	Requirement
10μf 106k025NLF	1 per board
cost per part × 1 =	
47μf 476K020WLG	1 per board
cost per part × 1 =	

Supplier: Mallory

8. Ferrite Core.

T80-1 Requirement: 1 per board

cost per part × 1 =

Supplier:

Amidon Associates
12033 Otsego Street
North Hollywood, CA 91607
(818) 760-4429

9. Mounting Screw.

4-40 × 1/4 Phillips pan head machine screw Requirement: 16 per board.

cost per part × 16 =

Supplier:

Bonneville Industry Supply Co.
45 So. 1500 W.
Orem, Utah
(801) 225-7770

10. Bannana Plug Jack.

H.H._Smith_Type	Order_#	Requirement
White 1509-101	28F1178	6/board-color your choice
Red 1509-102	35F870	6/board-color your choice
Black 1509-103	35F869	6/board-color your choice
Green 1509-104	28F1179	6/board-color your choice
Blue 1509-105	28F1180	6/board-color your choice
Yellow 1509-107	28F1182	6/board-color your choice

cost per part × 6 =

Supplier: Newark Electronics

11. Switch.

76P$B04 4-bit side actuated piano-dip Requirement: 1 per pin

cost per part × 24 =

Supplier: Grayhill Co.

12. Connectors - Snap-on SMB.

51-051-0000-220 - Straight jack receptacle Requirement: 2 per pin

cost per part × 48 =

Supplier: Sealectro

Test Fixtures for High-Speed Logic

AN203

13. Mounting frame.

Signetic's number CB-1.0		Requirement: 1 per test fixture
Supplier:	Electronic Chassis Corp. 468 North 1200 West Lindon, Utah 84062 (801) 785-9113	

14. Hookup wire.

No. 18/20 gauge Teflon coated — about 24 inches per test fixture.

The following components may be needed in use of the test fixtures but are not part of the test fixtures.

61-001-0000-89	50Ω terminator plug	As required or hand built with 50Ω resistor and 51-007-0000
51-007-0000	Straight Cable Clamp Type	As required
51-083-0000-222	"T" adaptor J-J-J	As required
51-085-0000	"T" adaptor J-P-J	As required
51-072-0000	Adaptor J-J	As required
51-073-0000	Adaptor P-P	As required
51-001-0020	Shorting plug	As required
61-002-0000-89	50Ω terminator jack	As required
Supplier:	Sealectro Corp (415) 965-1212	

Test Fixtures for High-Speed Logic

AN203

6. APPENDIX II-Construction Hints

A suggested order of assembly is as follows:

1. Cut traces for 450Ω resistor. (Not needed for ECL)
2. Install SMB Connectors. Elevate base from board .05″.
3. Install DIP Switches. Note: Numbers on switches may not correlate to Vs supply numbers.
4. Install Augat socket pin.
5. Install load/termination resistors and capacitors.
6. Strap V_{CC} and GND pins to appropriate bus strips.
7. Install bypass capacitors.
8. Clean flux off of board and components.
9. Check for lead to frame shorts on PLCC board. (Not discussed in App Note.)
10. Install banana jacks on frame.
11. Attach board to frame with 1/4 Phillips pan head machine screws.
12. Wrap wire 8-12 times around ferrite core. Leave enough wire to connect to frame and board. See Figure 1.
13. Connect V_{CC}, GND, and voltage supplies from banana jacks to board.
14. Remove all remaining flux. Keep "flux-off" from banana jacks.

Hints on construction:

— A .05″ shim that fits under the SMB connector base helps elevate it during construction.

— Mount the SMB connector with flat side out rather that point side out. See Figure 8.

— Solder Augat socket pins in with a part inserted to hold the pins steady.

— "Piano DIP" switches have the numbers reversed from the Board notation. Taping a new number on the board designations will help match the switches.

— Hint for solder chip components: apply a small amount of solder on one side of the pads on the board.

— Keep DIP switches and SMB connectors spaced as far away from each other as the holes will permit, ie., push the SMBs in and the DIP switches out.

Section 7
Surface Mounted ICs

Surface Mounted ICs

INTRODUCTION

Economic survival is driving the electronics industry to use cheaper, faster, more reliable and more dense systems and components. Assembly technologies, such as SMD (Surface Mounted Device) technology, developed and used in hybrids and for military electronics for over two decades, is being adapted to commercial electronics as part of this evolution. With SMD technology, components are soldered directly to a metalized footprint on the surface of the board or substrate rather than being inserted through holes drilled in the board and then soldered. Because of this evolution, package styles specially designed to facilitate surface mounting are now in high demand.

The reasons for the change to SMD technology vary from one customer to another; but the primary motivator is higher profits through lower manufacturing and material costs, an improved product, or both.

Improved Electrical Performance

Because SMD packages are much smaller than their DIP counterparts, they have much less capacitance and inductance, and provide improved AC performance, especially in high-speed environments. They help to minimize problems associated with ground bounce and multiple output switching found with standard DIP packages. The SO package is especially suitable for high-speed families such as FAST and High-Speed CMOS where package inductance can induce or compound problems not normally found in slower technologies.

Ease Of Automation

SMD pick-and-place machines offer higher yields, faster cycle rates (3 – 10x faster), and much higher throughput volumes than automatic insertion machines for DIP packages.

Greatly Increased Densities

Greatly increased densities can be achieved through surface mounting. The packages themselves are much smaller (as much as 70%) and can be placed much closer together. Furthermore, both sides of the board can be used with SMDs.

Reduced Board Costs

The number of layers, total size of the board, and the number of plated through holes can be reduced, thus lowering the total cost of the board (many companies claim savings of 30 to 50%).

Easier Board Rework

In those instances where rework is necessary, it is much faster and cheaper with SMDs.

Improved Reliability

Not only are the components proving to be at least as reliable as their DIP counterparts, surface mounted assemblies show fewer failures in stress tests than equivalent through hole assemblies.

Lower Shipping, Storage And Handling Costs

SMD components are up to 70% smaller and weigh up to 90% less than DIPs (up to 95% savings in storage area for Tape & Reel SMD components vs DIPs and up to 90% savings in component weight). Surface mount assemblies offer additional savings in both weight and space, both of which can be linked to increased profits.

SMD packages for integrated circuits fall into two categories: Swiss Outline, also known as Small Outline (SO), and the Plastic Leaded Chip Carrier (PLCC).

SO PACKAGE

The SO package was developed by N.V. Philips Corp, originally for the Swiss watch industry. In the mid 1970s Signetics introduced linear ICs in SO packages to the US market (hybrid and telecommunications). As demand grew, other technologies such as FAST, Low Power Schottky, Schottky, TTL, CMOS, High-Speed CMOS (HC and HCT), ECL, ROMs, RAMs, PROMs, were made available in SO packages.

The SO is a dual-in-line plastic package with leads spaced 0.050″ apart and bent down and out in a Gull-Wing format. It comes in two widths: 0.150″ SO, and 0.300″ SOL (SO-Large) depending on the pin count.

As ICs became more complex and the number of pins grew, the standard dual-in-line packages grew longer and wider, presenting new electrical and mechanical problems. Some of these were resolved with the introduction of the ceramic leadless chip carrier (LCC). These were square, ceramic packages without leads which can be socketed or soldered directly to a substrate if the thermal coefficient of expansion of the chip carrier and the substrate are to be matched.

In 1980, the Plastic Leaded Chip Carrier (PLCC) was introduced as a cheaper alternative to the LCC. However, this was at the same time that SMD was winning acceptance in commercial electronics and the PLCC was seen as an ideal SMD package for the higher pin count devices (those with more than 28 leads). The PLCC is a square, plastic package with leads on four sides, spaced down and under in a J-Bend configuration. It is available in the higher pin counts: 20, 28, 44, 52, 68, 84 with even higher pin counts under development.

The smallest square PLCC is the 20-pin package. There are many reasons for this; the primary one is that below 20 pins, the package would be as thick as it is square,

Table 1

PIN COUNT	SO	SOL	PLCC
8	x		
14	x		
16	x	x	
18		x	x (rectangular)
20		x	x
24		x	
28		x	x
44			x
52			x
68			x
84			x

Table 2. Maximum thermal Resistance (θ_{JA}) Values For SMD Packages (°CC/W)

PINS	SO	SOL	PLCC
8	160		
14	115		
16	110	90	
20		85	70
24		75	
28		70	60
44			42
52			39
68			42
84			32

resulting in a cube-like package which would be very difficult to handle in an automated environment.

Logic and linear devices are available in SO while the more complex parts such as microprocessors, microcontrollers, complex peripherals, large memory devices, and other higher pin count integrated circuits will be found in the PLCC.

ASSEMBLY

The assembly of these SMD packages is virtually the same as for the older DIP packages using the same materials and most of the same equipment and assembly technologies.

The only differences in the process are the smaller lead frames, different lead bends (gull-wing for SO and J-Bend for the PLCC), and closer spacing resulting in a much smaller package for the same basic die.

RELIABILITY

Reliability studies of SMD components, conducted not only by Signetics and Philips, but by many of our competitors and customers, have revealed that these packages are at least as reliable as the standard plastic DIP packages that have been used over the past 20 years. In several cases, test results of the SMD packages have been better than their DIP counterparts.

THERMAL CHARACTERISTICS

Thermal characteristics of ICs have always been a major consideration to producers and users of electronics products because an increase in junction temperature (T_j) can have an adverse effect on the long term operating life of an IC. The advantages realized by miniaturization have trade-of in terms of increased junction temperatures. Some of the variables affecting T_j are controlled by the producer of the IC, while others are controlled by the user and the environment in which the device is used.

With the increased use of SMD, thermal management remains a valid concern because not only are the packages much smaller, but the thermal energy is concentrated much more densely on the PCB. For these reasons users of SMD must be ore aware of all the variables affecting T_j.

POWER DISSIPATION

Power dissipation (P_D) varies from one device to another depending on technology and complexity. It can be obtained by multiplying V_{CCmax} by the I_{CC} Characterized at the maximum ambient temperature expected (in the case of TTL, 70°CC).

- Junction temperature (T_J) is the temperature of a powered IC measured at the substrate diode. When the device is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A).
- All standard TTL, Schottky, Low Power Schottky, and FAST being built by Signetics use copper leadframes.
- The ability of the package to conduct heat from the chip to the environment is expressed in terms of thermal resistance, normally called Theta JA (θ_{JA}). θ_{JA} is the total resistance from the junction to ambient and is often separated into two components: θ_{JC} (junction to case) and θ_{CA} (case to ambient). $\theta_{JA} = \theta_{JC} + \theta_{CA}$ θ_{JA} values for SMD packages are listed in Table 2.
- All measurements are in still air.
- $T_{A\ MAX}$ is +70°C.
- I_{CC} characterized at nominal V_{CC} and +70°CC ambient.
- Calculate power (P) by multiplying V_{CC} nominal × I_{CC} at +70°CC.
  $P = I_E$
- Calculate rise in (T_J) by multiplying Power by θ_{JA}.
  $T_J = P \times \theta_{JA}$
- Add $T_J + T_{A\ MAX}$. If result is greater than 120°CC, then thermal mounting or some other way to reduce the T_J must be used.

Factors Affecting Thermal Resistance

In addition to possible loading and duty cycle factors in some technologies, there are several factors with affect θ_{JA} of any IC package. Effective thermal management demands a sound understanding of all these variables.

Package variables include the leadframe design, leadframe material, the plastic used to encapsulate the device, and to a lesser extent, other variables such as the die size and die attach methods. While the thermal conductivity of the wire can be calculated, it is too insignificant to be considered as a factor.

Other factors that have a significant impact of the θ_{JA} include the substrate upon which the package is mounted, the density of the layout, the gap between the package and substrate, the number and length of traces on the surfaces of the board, the use of thermally conductive epoxies, and any external cooling methods.

STANDARDIZATION

The SO package is an industry standard format. In June 1985, the JEDEC (Joint Electronics Engineering Council) of the EIA (Electronics Industries Association) issued a Solid State Product Outlines Standard for each of the SO formats: MS-012 AA-AC for the 0.150" body width SO and Ms-013 AA-AE for the 0.300" body width SOL. In addition to the JEDEC Standard, de facto standardization has been achieved in the industry in that most of the major US and European IC manufacturers (more than 15 companies currently) use this standard.

The PLCC is also a standardized format, with a JEDEC REgistered Outline #MO-047 AA-AH. It also is multiple sourced with over 10 US IC manufacturers using this standard.

Points worth noting: ALL SO AND SOL PACKAGES HAVE 0.050" LEAD SPACING A GULL-WING LEAD BEND, WHILE ALL PLCC PACKAGES HAVE THE SAME LEAD SPACING AND A J-BEND LEAD BEND.

TAPE AND REEL

One revolutionary phenomenon in SMD is the development of Tape and Reel for the IC packages. Philips and several other companies making automatic placement equipment recognized the need for a feed system which allows for positive indexing large volumes of components at high-speed in order to get maximum efficiency out of the new pick-and-place machines. Tubes are limited to a relatively small number of parts (dictated by tube length) and depend on gravity to feed components to the placement head. After several proposed tape formats, Philips, Signetics, many of the component and placement equipment manufacturers, and board manufacturers convened under the auspices of EIA (Electronic Industries Association) and agreed on an industry standard specification for Tape and Reel for both SO and PLCC packages. The proposed EIA specification RS 481A is being used by Signetics and

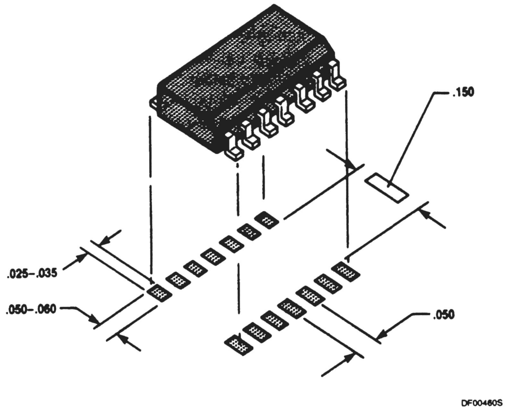
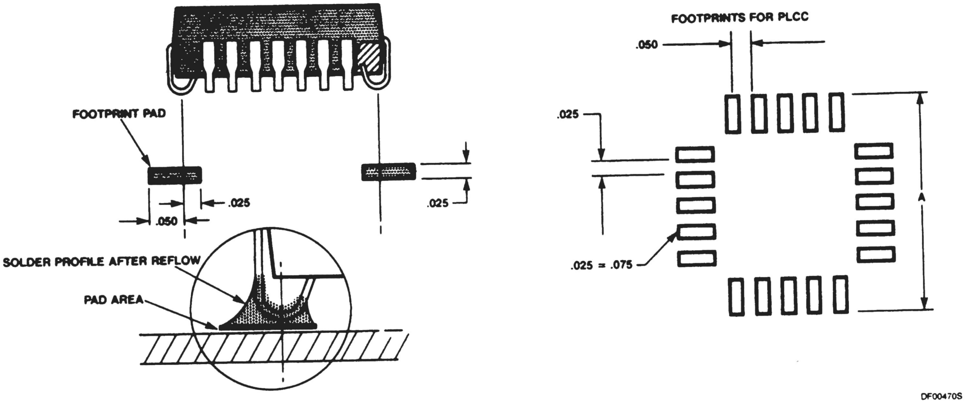

.150
.025–.035
.050–.060
.050
DF00460S

Figure 1. Manufacturers' Recommended Footprint


FOOTPRINTS FOR PLCC
.050
.025
.025 = .075
A
FOOTPRINT PAD
.025
.050
.025
SOLDER PROFILE AFTER REFLOW
PAD AREA
DF00470S

PINS	A
20	.425
28	.525
44	.725
52	.825
68	1.025

Figure 2. Footprint Design for The PLCC-IC

Philips, both of whom have shipped components on Tape and Reel since late 1984.

SUCCESS IN SURFACE MOUNTING BEGINS WITH THE DESIGNER

In addition to the different package configurations, surface mounting is done on a much smaller scale. Instead of the plated through holes, metalized footprints must be etched onto the substrate surface.

The designer will be using a ore refined set of rules for layout of the surface mount PC board. Because the components can be spaced closer together with small contact spacing, a narrower conductor trace width is necessary. A common signal conductor can be 0.010″ to 0.012″ wide and 0.015″ through 0.030″ is adequate for power and ground bussing. The suggested footprint contact area has a generous tolerance. For the SO I.C.,a rectangular pattern is used on 0.050″ spacing. The length of the pad is 0.050″ to 0.060″ and the width can vary from 0.020″ to 0.035″. The 0.025″ × 0.050″ footprint pattern will work well using the grid placement system favored by most designers. The 0.012″ conductor width spaced at 0.025″ provides a reasonable 0.013″ air gap between traces. However, if conductor pads, it will be necessary to neck down the trace width to 0.008″ and still retain an equal airgap at each side. Because neck down traces require additional time in both hand taping or CAS/photo plot generation of artmasters, some compromises may be justified. By reducing the contact pad size to.0.020″ × 0.050″, it is possible to route a consistent 0.010″ conductor trace width and still maintain the desired clearances. However, some PC board shops may not maintain the consistent quality necessary when using this fine line approach over the entire board. It is important to discuss limitation and premium cost penalties with your supplier before full commitment to the 0.010″, and smaller, trace widths.

Another very important consideration to be taken into account is the thermal concentration caused by miniaturization. The same die is being used in the SMD as in the DIP, thus the power dissipated is the same; however, the smaller packages are being placed much closer together, concentrating the thermal energy. The trde-offs between the increase in density and the concentration of thermal energy must be evaluated by the board manufacturer.

These factors may influence the choice of PCB material, the number of layers, and the thickness of the PCB board. New methods to transfer heat from the package to the board and then away from the board should be considered by the designer.

Other factors to be considered are the placement system, soldering method, post-assembling cleaning, inspection, test, and the availability of parts in SMD packages.

One of the first steps is to list all the devices needed and to determine which ones are available in SMD format. With the growth of popularity of SMD, the number of different functions offered by Signetics continues to grow rapidly. In addition to the SIGNETICS SMD POCKET GUIDE, there are several cross-reference lists available from design and assembly services. However, with the explosive growth of this market NONE OF THESE LISTS ARE NECESSARILY CURRENT. Please check with your local sales office because the parts availability lists are growing almost daily.

When choosing the type of footprints to use, it is very important that the designer considers the soldering method being used.

Basically there are two types of soldering in use today: flow soldering (wave, drag, or hot solder dip) an reflow soldering (vapor phase, infrared, thermal conduction through the PCB, and hot air).

The SO package can be soldered using a flow soldering method. The devices must be attached to the PCB by means of an adhesive because the device side of the board will be facing down as it goes through the solder wave. The orientation of the part as it goes through the solder wave can play an important role in the elimination of bridges. Experiments should be conducted by the user to determine the best footprints for use in a particular soldering system. Some users feel that the narrow footprints help to reduce solder bridges. Others have been experimenting with rounded footprints to reduce bridging during wave soldering and claim to have had very good results.

Reflow soldering has been done for many years in the hybrid industry. A solder paste or solder cream is applied to the footprint prior to placement of the component. These pastes an creams contain tiny spheres of solder suspended in a carrier which contains the flux. As the substrate temperature is raised, the flux, solvents, and carriers are driven off and the solder liquifies. Various melting point pastes and creams are available. As the liquid solder migrates to the metallized footprints, the surface tension is enough to move the leaded components. For SO packages, this can be an advatage because it acts as a self-positioning mechanism. However, it can be a problem for the smaller passive components if the solder paste isn't printed on evenly. If there is an uneven amount of solder paste on one end of one of these smaller devices, the surface tension can pull stronger on one side causing a "tombstoning" effect, i.e., one end of the device is lifted straight up.

Many variations of footpring patterns are possible. The formula shown in Figure 1 is applicable for both reflow and wave solder processes. Many configurations are possible

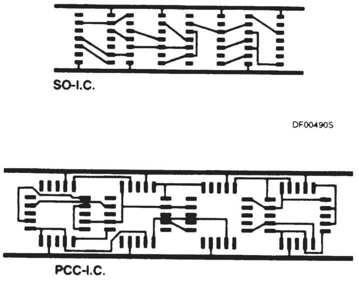


Figure 3. Planning – Layout And Component Placement

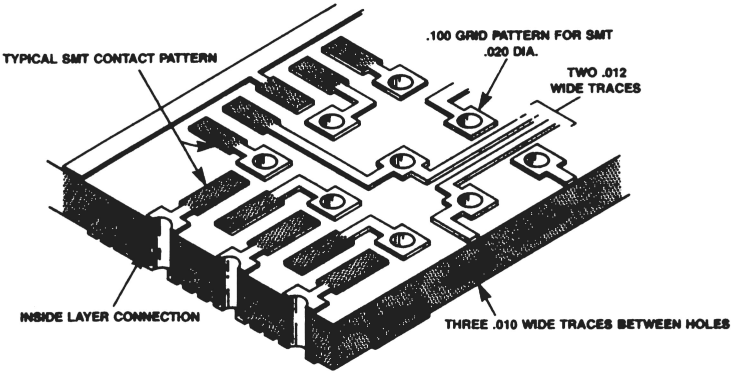

TYPICAL SMT CONTACT PATTERN
.100 GRID PATTERN FOR SMT
.020 DIA.
TWO .012
WIDE TRACES
INSIDE LAYER CONNECTION
THREE .010 WIDE TRACES BETWEEN HOLES
DF005108

Figure 4

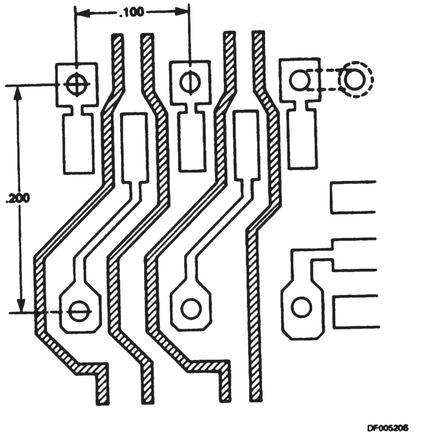

.100
.200
DF005208

Figure 5

and should be tried on an experimental basis before commitment to a large production run. Both time and development costs can be conserved by utilizing design and process consultants specializing in surface mount technology.

Figures 1 and 2 show some typical footprints used in reflow soldering. Note that the width of the footprint for the SO package varies from 0.025″ to 0.035″. Most users tend towards the narrow footprint. Further, the length to these prints should be kept as short as possible to prevent the part from swimming or sliding back and forth on the footprint while still allowing a good meniscus.

Another factor worth noting is that the footprint for PLCC should not extend too far under the package as this could promote solder bridges under the package where they can not be seen during inspection. The footprint for the PLCC should extend out further from the package than the lead itself to allow a good meniscus that will result in a strong, inspectable bond.

Careful placement of related components will allow a more effective use of a much smaller surface area. The interconnections that can be made on the substrate surface result in the elimination of feedthrough holes. Reduction of these holes and their associated pad areas further increase the density of the layout, and reduce total board cost as well. As indicated, the SO package has the same pinout on two parallel rows as found on the older DIP packages being replaced. Arranging related ICs in blocks or functional clusters with their associated discreet components can also help to maximize the use of the available surface area.

For several reasons, many users have expressed their preference for SO format through 28 pins. The SO is much smaller and lighter than the PLCC. The SOI, although a bit longer than the PLCC, still occupies about the same board space.

Further, when using several packages and connecting them together, a given number of SO and SOL packages would take much less space than the same number of PLCCs, simply because of the interconnect geography. (See Figure 3).

Besides being smaller, the SO format is dual-in-line and has the same pinouts as those of a standard DIP (PLCC pinouts vary between devices as well as between manufacturers). The SO format is easier to handle and is much easier to visually inspect.

For devices over 28 pins, the PLCC is the package of choice, largely because it can hold a much larger die than the 0.300″ wide SO packages.

In the early days of PCB technology when plated through holes were not possible, designers were forced to carefully plan component arrangements and connections. Using experience and ingenuity, they were able to eliminate crossovers while reducing the need for unwanted jumpers. With the advent of plated through holes and multilayer boards, the restriction to single sided boards was eliminated. Using the single sided concept the techniques used to interconnect the SMDs are as important as the footprint patterns. As noted before, the contact pads on 0.050″ centers, range between 0.025″ and 0.035″ in width. Prior to choosing to add a feedthrough hole on the pad itself, two factors should be considered: 1) The hole diameter selected must allow for a reasonable location tolerance. A 0.010″ to 0.015″ diameter plated through hole in 0.062″ thick FR4 material may increase the cost of your PCB. 2) Unless the feedthrough hole on the footprint area is either plugged or masked, in a reflow soldering situation, the solder will tend to migrate away from the IC contact resulting in a poor solder joint.

It is more desirable to add a separate pad for via or feedthrough requirements. To further provide for routing conductor traces while insuring an acceptable air gap, you may choose to use a 0.035″ to 0.037″ square pad for these feedthrough holes. The square configuration will furnish more than enough metal in the diagonal corners to compensate for the reduced annular cross section at the sides of the square. The 0.035″-0.037″ square feedthrough pad can be spaced at 0.050″ when necessary or on the more traditional 0.100″ pad. With this spacing it is possible to route two 0.012″ wide conductor traces between pads, something only possible before with costly multilayer designs using leaded through hole technology.

The feedthrough pad is then connected to the component contact area with a narrow trace. This narrow trace reduces migration of the solder paste during the reflow process. To further reduce migration of the liquid solder, application of solder mask coating over surface areas not requireing solder is recommended. This coating is applied with a wet screen process or photographically as a dry film and will act as a dam to contain solder to the contract area. (See Figures 4 and 5).

When using reflow soldering, the trace width should be about half the width of the footprint pattern. As noted before the signal carrying conductors are generally 0.012″ to 0.015″ wide. Supply voltages are carried on wider traces. When running traces between the device leads, it will be necessary to reduce the width to about 0.008″ which provides an 0.008″ gap between the trace and the edge of the pads when using 0.025″ pads.

Because the SMDs are so much smaller than their leaded counterparts, the scale of the layout should be considered. On larger boards with a mix of SMDs and leaded devices, a 2:1 scale may be adequate. More complex layouts can be designed at 4:1 scale with excellent results. The larger scale will make it possible to increase density while assuring accuracy. If designing with a CAD system, accuracy and density can both be increased by increasing the grid resolution. Routing conductor traces will require careful planning, it is customary to use a 90° or 45° angle (Figure 6) when traces must divert from a continuous line.

Offset stepping several 0.012″ wide conductor traces on 0.025″ spacing will require necking down at the point of direction change to maintain the desired air gap. The start and stop points of photoplotter aperture runs must be carefully executed to reduce the chance of overlay and shorting. if outside services are used for digitizing or photoploting, discuss your requirements for accuracy before proceeding. Some compromises may have to be made to insure quality and control costs. Preparing artmasters on mylar using precision tape products and pre-printed footprint patterns may afford more flexibility during your entry into SMD technology. Changes can be mad easily, and economical photo reduction processes will provide high quality working film. The technique used to prepare working film is a choice generally influenced by in-house capability or services available in a region.

Dramatic changes are taking place throughout this industry. Surface mount technology is key to an efficient transition into miniaturization and automation of electronic production.

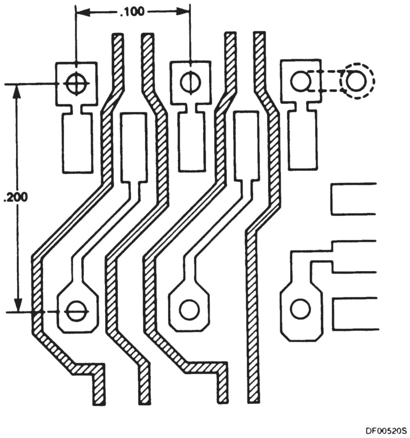

.100
.200
DF00520S

Figure 6

Section 8
Package Outlines

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Package Outlines for Hermetic CERDIP . . . .

Package Outlines

PACKAGE OUTLINES FOR PLASTIC PACKAGES

The following information applies to all plastic packages unless otherwise specified on individual package outline drawings.

1. Dimensions are shown in Metric units (Millimeters) and English units (Inches).
2. Lead material: Copper Alloy, solder (63%Sn/37%Pb) dipped.
3. Body material: Plastic (Epoxy)
4. Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. The substrate diode of a Bipolar technology device is generally the diode used in these tests. Die size and test environment have significant effects on thermal resistance values.

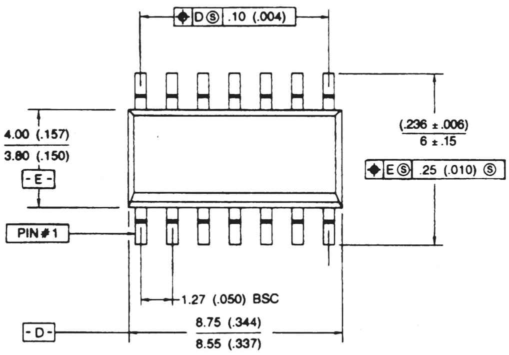
PLASTIC PACKAGES OUTLINES

Package Type	Number of Leads	Package Feature	Package Ordering Code	Package Outline Code	Thermal Resistance θ_{JA}/θ_{JC} (°C/W)	Die Size (square mils)	Test Conditions	
							Test Ambient	Test Fixture
SO[1] (Copper Leadframe)	14-pin (SO-14)	3.9mm (0.15″) Body width	D	DH1	124/37	2,500	Still air at room temperature	Device soldered to Philips glass epoxy test board (1.12″ × 0.75″ × 0.059″) with 0.008 – 0.009″ stand-off. Accuracy: ± 15%
	16-pin (SOL-16)		D	DJ1	113/36			
	20-pin (SOL-20)	7.5mm (0.30″) Body width	D	DL2	90/28	5,000		Device soldered to Philips glass epoxy test board (1.58″ × 0.75″ × 0.059″) with 0.008 – 0.009″ stand-off. Accuracy: ± 15%
	24-pin (SOL-24)		D	DN2	76/26			
DIP[2] (Copper Leadframe)	14-pin (DIP-14)	0.300″ Lead row centers	N	NH1	89/44	2,500	Still air at room temperature	Device in Textool ZIF socket with 0.040″, stand-off. Accuracy: ± 15%
	16-pin (DIP-16)		N	NJ1	86/43			
	20-pin (DIP-20)		N	NL1	74/32	5,000		Device in Textool ZIF socket with 0.040″, stand-off. Accuracy: ± 15%
	24-pin SLIM DIP (DIP-24)		N	NN1	65/36			

NOTES:

1. SO = Small Outline
2. DIP = Dual-In-Line Package

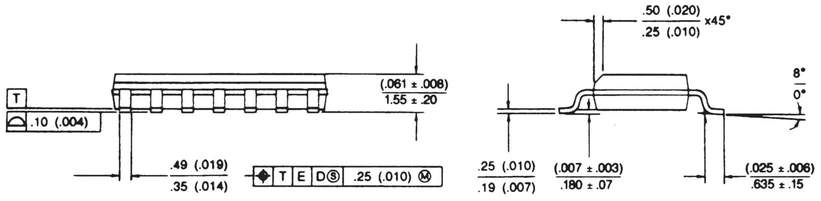
14–PIN PLASTIC SO



⌖ D Ⓢ .10 (.004)
4.00 (.157)
3.80 (.150)
-E-
PIN #1
(.236 ± .006)
6 ± .15
⌖ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
8.75 (.344)
8.55 (.337)

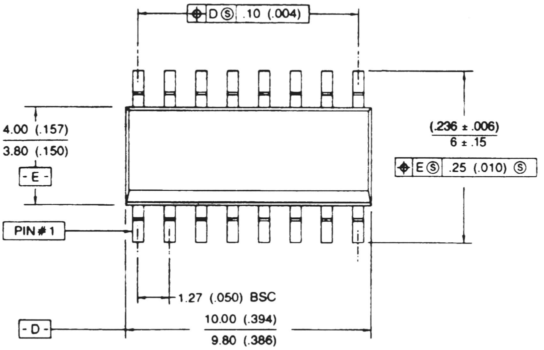
NOTES:

1. Packaging dimensions conform to JEDEC specification MS–012–AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M– 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



T
⌓ .10 (.004)
(.061 ± .008)
1.55 ± .20
.49 (.019)
.35 (.014)
⌖ T E D Ⓢ .25 (.010) Ⓜ
.50 (.020)
.25 (.010)
x45°
8°
0°
.25 (.010)
.19 (.007)
(.007 ± .003)
.180 ± .07
(.025 ± .006)
.635 ± .15

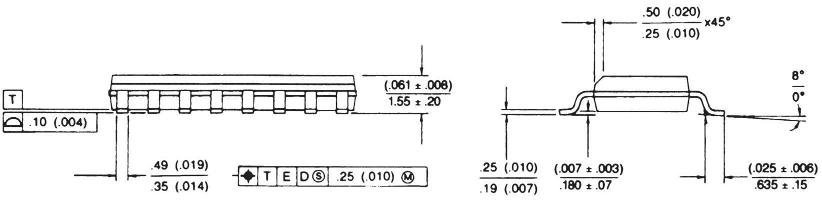
16–PIN PLASTIC SO



⌖ D Ⓢ .10 (.004)
4.00 (.157)
3.80 (.150)
-E-
PIN #1
(.236 ± .006)
6 ± .15
⌖ E Ⓢ .25 (.010) Ⓢ
1.27 (.050) BSC
-D-
10.00 (.394)
9.80 (.386)

NOTES:

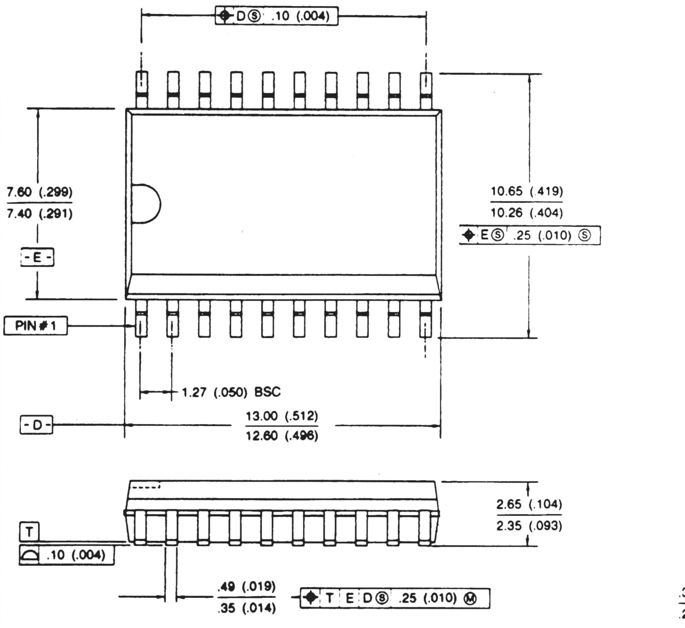
1. Packaging dimensions conform to JEDEC specification MS–012–AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M– 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



T
⌓ .10 (.004)
(.061 ± .008)
1.55 ± .20
.49 (.019)
.35 (.014)
⌖ T E D Ⓢ .25 (.010) Ⓜ
.50 (.020)
.25 (.010)
x45°
8°
0°
.25 (.010)
.19 (.007)
(.007 ± .003)
.180 ± .07
(.025 ± .006)
.635 ± .15

Package Outlines

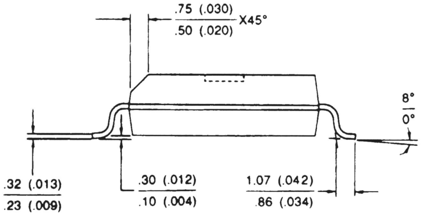
20–PIN PLASTIC SOL



D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
10.65 (.419)
10.26 (.404)
E Ⓢ .25 (.010) Ⓢ
PIN #1
1.27 (.050) BSC
-D-
13.00 (.512)
12.60 (.496)
2.65 (.104)
2.35 (.093)
T
.10 (.004)
.49 (.019)
.35 (.014)
T E D Ⓢ .25 (.010) Ⓜ

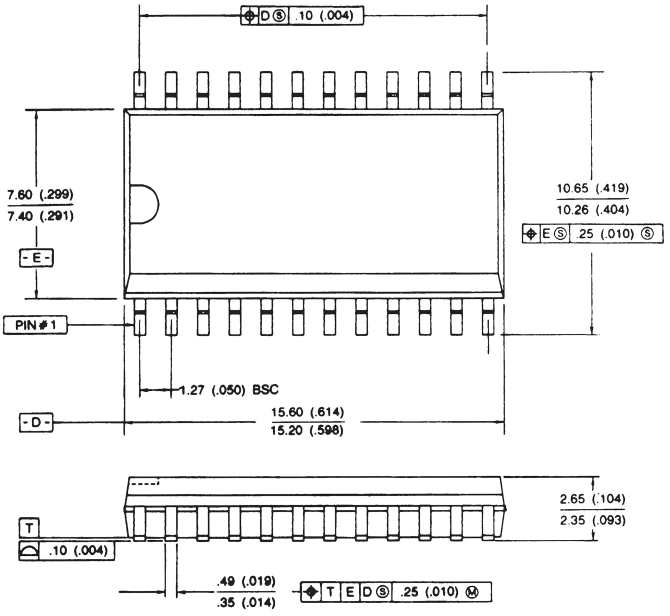
NOTES:

1. Packaging dimensions conform to JEDEC specification MS–012–AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M– 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



.75 (.030)
.50 (.020)
X45°
8°
0°
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
.86 (.034)

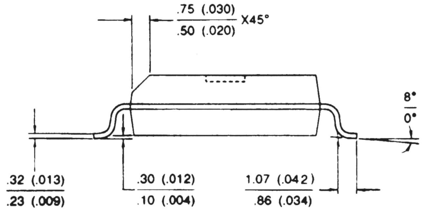
24–PIN PLASTIC SOL



D Ⓢ .10 (.004)
7.60 (.299)
7.40 (.291)
-E-
10.65 (.419)
10.26 (.404)
E Ⓢ .25 (.010) Ⓢ
PIN #1
1.27 (.050) BSC
-D-
15.60 (.614)
15.20 (.598)
2.65 (.104)
2.35 (.093)
T
.10 (.004)
.49 (.019)
.35 (.014)
T E D Ⓢ .25 (.010) Ⓜ

NOTES:

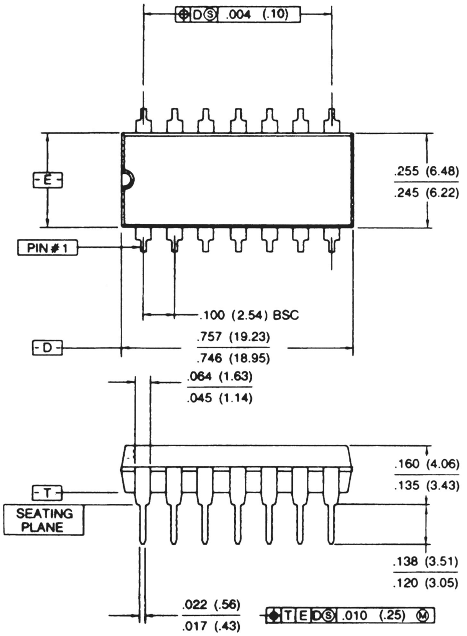
1. Packaging dimensions conform to JEDEC specification MS–012–AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M– 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



.75 (.030)
.50 (.020)
X45°
8°
0°
.32 (.013)
.23 (.009)
.30 (.012)
.10 (.004)
1.07 (.042)
.86 (.034)

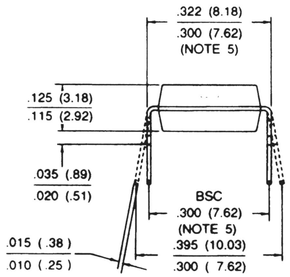
Package Outlines

14–PIN PLASTIC DIP

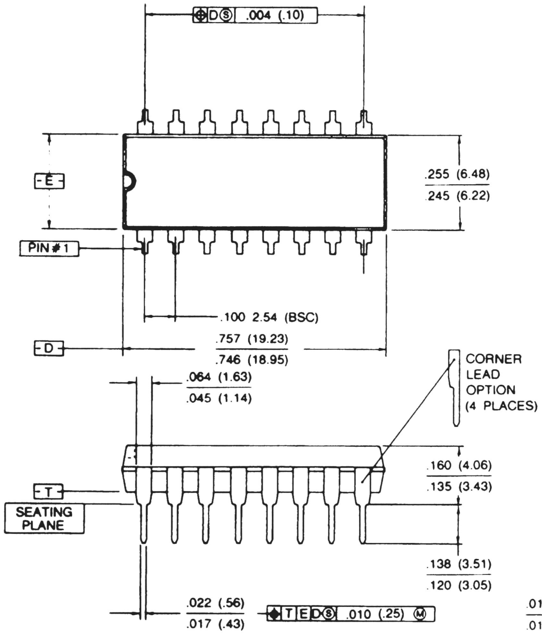

⊕ D Ⓢ .004 (.10)
-E-
.255 (6.48)
.245 (6.22)
PIN # 1
.100 (2.54) BSC
-D-
.757 (19.23)
.746 (18.95)
.064 (1.63)
.045 (1.14)
.160 (4.06)
.135 (3.43)
-T-
SEATING PLANE
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ

NOTES:

1. Packaging dimensions conform to JEDEC specification MS–012–AB for standard small outline (SO) package, 14 leads, 3.75mm (.150') body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M– 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

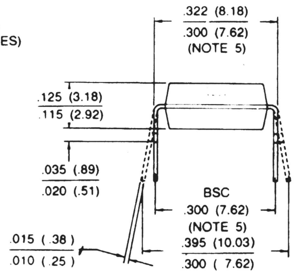

.322 (8.18)
.300 (7.62)
(NOTE 5)
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 5)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)

16–PIN PLASTIC DIP


⊕ D Ⓢ .004 (.10)
-E-
.255 (6.48)
.245 (6.22)
PIN # 1
.100 2.54 (BSC)
-D-
.757 (19.23)
.746 (18.95)
CORNER
LEAD
OPTION
(4 PLACES)
.064 (1.63)
.045 (1.14)
.160 (4.06)
.135 (3.43)
-T-
SEATING PLANE
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
⊕ T E D Ⓢ .010 (.25) Ⓜ

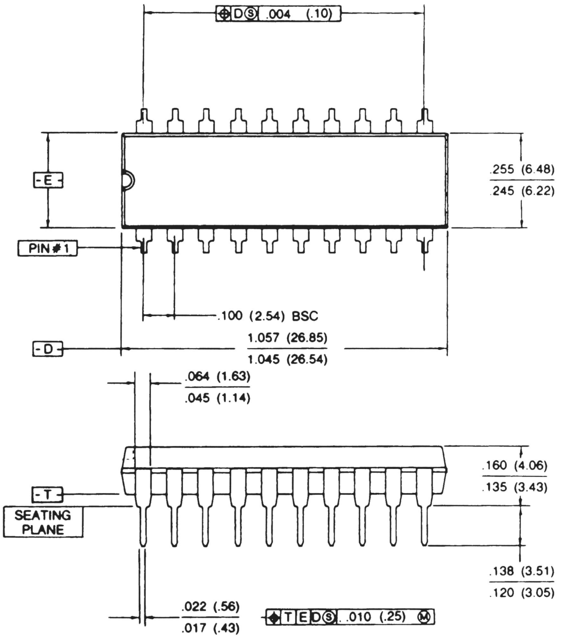
NOTES:

1. Packaging dimensions conform to JEDEC specification MS–012–AB for standard small outline (SO) package, 14 leads, 3.75mm (.150') body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M– 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.


.322 (8.18)
.300 (7.62)
(NOTE 5)
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 5)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)

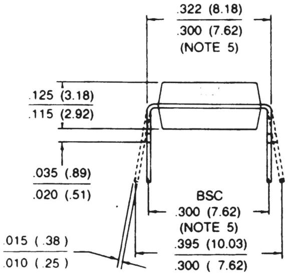
Package Outlines

20–PIN PLASTIC PDIP

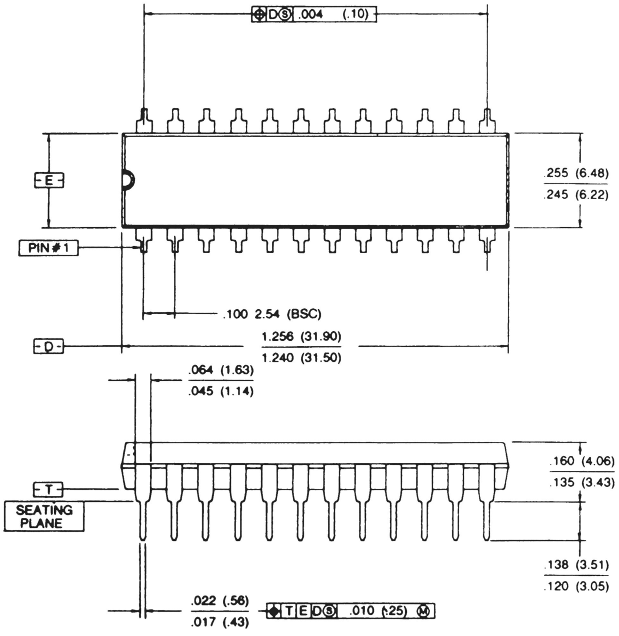

D S .004 (.10)
-E-
PIN #1
.255 (6.48)
.245 (6.22)
.100 (2.54) BSC
-D-
1.057 (26.85)
1.045 (26.54)
.064 (1.63)
.045 (1.14)
-T-
SEATING PLANE
.160 (4.06)
.135 (3.43)
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
T E D S .010 (.25) M

NOTES:

1. Packaging dimensions conform to JEDEC specification MS–012–AB for standard small outline (SO) package, 14 leads, 3.75mm (.150') body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M– 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

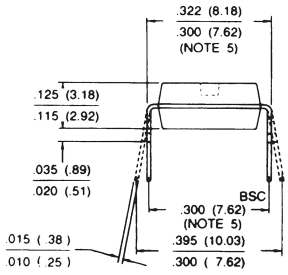

.322 (8.18)
.300 (7.62)
(NOTE 5)
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 5)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)

24–PIN PLASTIC PDIP


D S .004 (.10)
-E-
PIN #1
.255 (6.48)
.245 (6.22)
.100 2.54 (BSC)
-D-
1.256 (31.90)
1.240 (31.50)
.064 (1.63)
.045 (1.14)
-T-
SEATING PLANE
.160 (4.06)
.135 (3.43)
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
T E D S .010 (.25) M

NOTES:

1. Packaging dimensions conform to JEDEC specification MS–012–AB for standard small outline (SO) package, 14 leads, 3.75mm (.150') body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M– 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.


.322 (8.18)
.300 (7.62)
(NOTE 5)
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 5)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)

NOTES

NOTES

NOTES

NOTES

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MATERIALS*

The contents of each series are listed on pages III to VIII.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

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* Will replace the Components and materials (green) series of handbooks.

** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05	**Advanced Low-power Schottky (ALS) Logic Series**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
Supplement to IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers** NMOS, CMOS
IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom** Bipolar, MOS Radio pagers Mobile telephones ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**

DISCRETE SEMICONDUCTORS

This series of data handbooks comprises:

current code	new code	handbook title
S1	**SC01**	**Diodes** High-voltage tripler units
S2a	**SC02***	**Power diodes**
S2b	**SC03***	**Thyristors and triacs**
S3	**SC04***	**Small-signal transistors**
S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07***	**Small-signal field-effect transistors**
S6	**SC08***	**RF power transistors**
	SC09	**RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8a	**SC11***	**Light emitting diodes**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
S10	**SC14***	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**
S14	**SC18***	**Liquid crystal displays and driver ICs for LCDs**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T8	**DC01**	**Colour display systems**
T16	**DC02**	**Monochrome tubes and deflection units**
C2	**DC03***	**Television tuners, coaxial aerial input assemblies**
C3	**DC04***	**Loudspeakers**
C20	**DC05***	**Wire-wound components for TVs and monitors**

* These handbooks are currently issued in another series; they are not yet issued in the Display Components series of handbooks.

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
C14	**PA01**	**Electrolytic capacitors; solid and non-solid**
C11	**PA02***	**Varistors, thermistors and sensors**
C12	**PA03***	**Potentiometers, encoders and switches**
C7	**PA04***	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06***	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08***	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T1	*	Power tubes for RF heating and communications
T2a	*	Transmitting tubes for communications, glass types
T2b	*	Transmitting tubes for communications, ceramic types
T3	PC01**	High-power klystrons
T4	*	Magnetrons for microwave heating
T5	PC02**	Cathode-ray tubes
T6	PC03**	Geiger-Müller tubes
T9	PC04**	Photo and electron multipliers
T10	PC05**	Plumbicon camera tubes and accessories
T11	PC06	Microwave diodes and sub-assemblies
T12	PC07	Vidicon and Newvicon camera tubes and deflection units
T13	PC08	Image intensifiers
T15	PC09**	Dry reed switches
C8	PC10	Variable mains transformers; annular fixed transformers
	PC11	Solid state image sensors and peripheral integrated circuits

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* These handbooks will not be reissued.

** Not yet issued with the new code in this series of handbooks.

MATERIALS

This series of data handbooks comprises:

current code	new code	handbook title
C4 **C5**	**MA01***	**Soft Ferrites**
C16	**MA02****	**Permanent magnet materials**
C19	**MA03****	**Piezoelectric ceramics**

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* Handbooks C4 and C5 will be reissued as one handbook having the new code MA01.

** Not yet issued with the new code in this series of handbooks.

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